第五讲：存储器以及地址分配

1、TMS320F28335存储器空间分配

2、TMS320F28335存储器保护特点

3、XINTF接口

4、相关寄存器介绍

TMS320F28335存储器空间分配

时钟越快，处理基本逻辑运算的速度越快，处理过程中处理对象（数据）以及处理方法（指令）这些信息都要合理地存放与读取，存放这些信息的存储器以及存储器架构也是影响控制器速度与性能的重要指标。就像我们购买计算机时，除了关注CPU的主频外，还关注存储器的配置情况，例如内存的大小、硬盘的大小。

20世纪30年代中期，美国天才科学家冯·诺依曼大胆提出：抛弃十进制，采用二进制作为数字计算机的数制基础。

由于指令和数据都是二进制码，指令和操作数的地址又密切相关，因此，当初选择指令与数据存储在一起，经由同一总线传输是很自然的。

TMS320F28335存储器空间分配

但是，这种指令和数据共享同一总线的结构，取指令和存取数据要从同一个存储空间存取，经由同一总线传输，因此它们无法重叠执行，只有一个完成后再进行下一个，使得信息流的传输成为限制计算机性能的瓶颈，影响了数据处理速度的提高。

于是哈佛人提出了指令存储和数据存储分开的存储器结构，可以同时读取指令和数据，大批量处理数据的时候效率显著提高，即哈佛结构。

改进的哈佛结构一是允许数据存放在程序存储器中，并被算术运算指令直接使用，增强了芯片的灵活性；二是指令存储在高速缓冲器中，当执行此指令时，不需要再从存储器中读取指令，节约了一个指令周期的时间。

TMS320F28335存储器空间分配

F28335 DSP就是采用多级流水线的增强的哈佛总线结构，能够并行访问程序和数据存储空间。多级流水线指同时将指令的基本操作，分解为几个基本操作，这些元操作可以流水执行，并且对程序进行分支预测，进行多级流水线操作，使得数据处理的效率大大提高。

在F28335芯片内部集成了大量的不同的存储介质，F28335片上有256K×16位的FLASH，34K×16位的SARAM，8K×16位的BOOT ROM，2K×16位的OPT ROM，采用统一寻址方式（程序、数据和I/O统一寻址），从而提高了存储空间的利用率，方便程序的开发。

除此之外，F28335 DSP还提供了外部并行扩展接口XINTF，可进一步外扩存储空间。

TMS320F28335存储器空间分配

F28335的CPU内核本身并不包含任何存储器，通过总线访问芯片内部集成的或者外部扩展的存储器。其总线按照改进哈佛结构，分成了32位的数据读、数据写数据总线，地址读、地址写总线，公用数据总线即程序总线，包括22位的程序地址总线，用于传送程序空间的读/写地址，32位读数据程序总线，用于读取程序空间的指令或者数据。

改进的哈佛结构其实是综合了冯·诺依曼结构的简洁，哈佛结构的高效。F28335应用32位数据地址和22位程序地址控制整个存储器以及外设，最大可寻址4M字的数据空间和4M字程序空间。

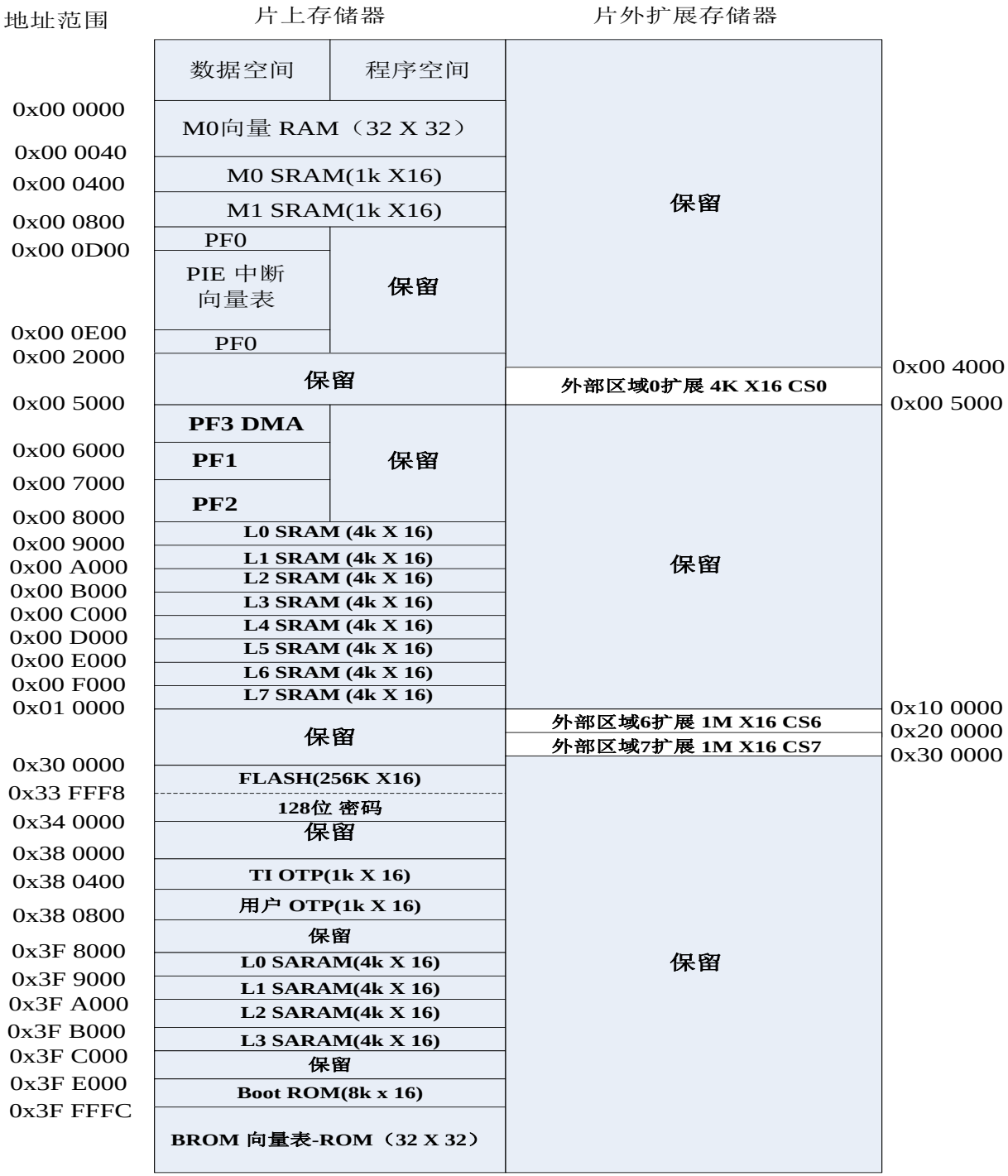


图5.1是F28335处理器的存储器配置及地址映射。

图5.1的映射表就像是各个空间的地图一样，有些空间既可以作为数据空间也可以作为程序空间，有些空间只能作为数据空间，有些空间是受到密码模块保护，有些空间地址是作为保留的，具体内容就要仔细对照这个地图来进行查阅了。

受到密码模块保护的空间存放的寄存器不可以随便配置，若要对存放在受到密码模块保护空间内的寄存器进行配置，要进行EALLOW声明，以EDIS结束声明，起到保护和警示作用。

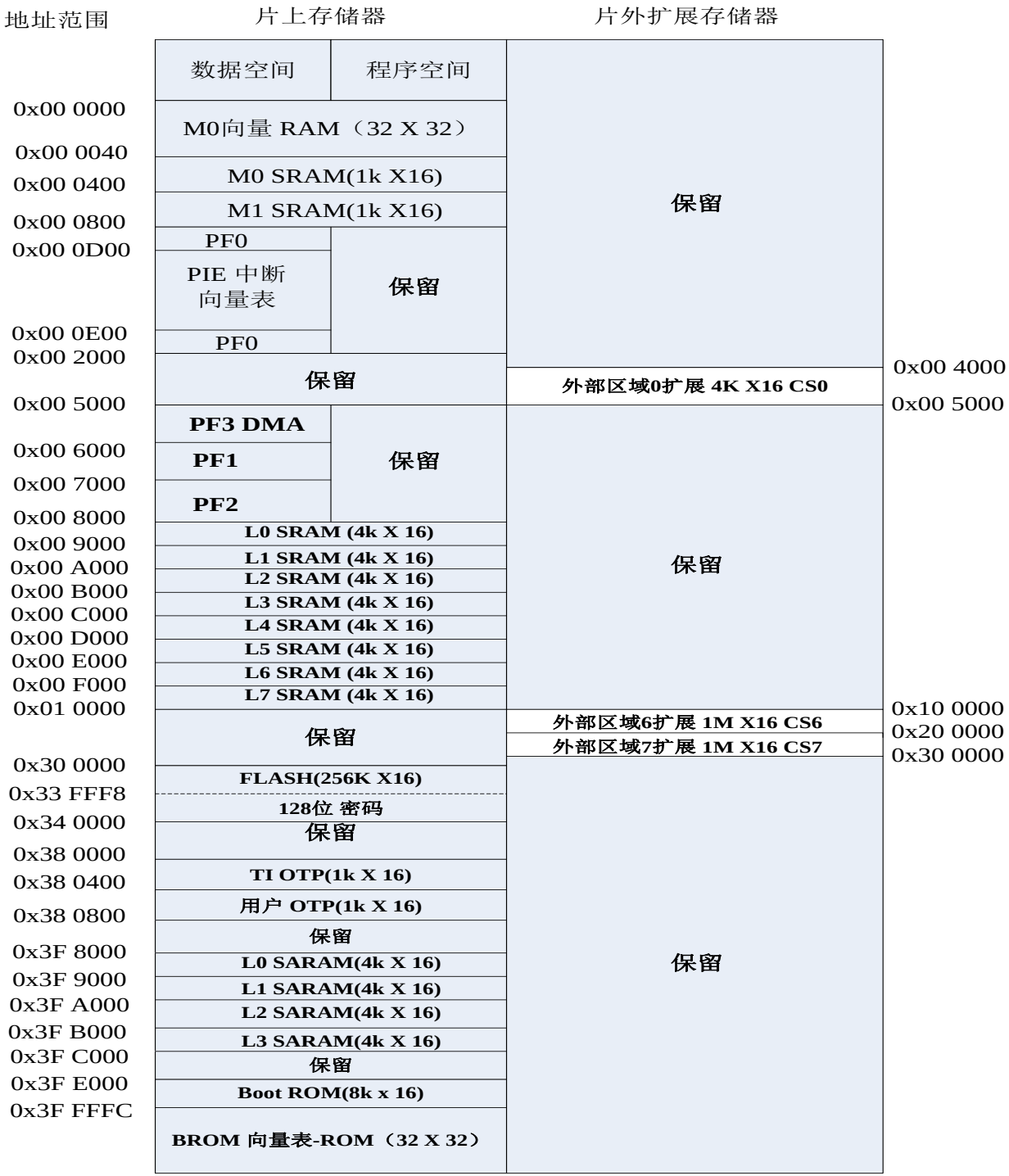


图5.1右半部分主要是通过XINTF外扩的存储空间，当片内数据存储空间不够的时候，我们可以外扩存储器。其中的保留区是为片内存储器所占的地址。

F28335对数据空间和程序空间进行了统一编址。F26335的各存储器地址都是连续编码的，且空间地址是唯一的。

图5.1左半部分，首先对M0 SRAM从0X000000开始编码一直到0X000400结束，可以计算出这是1K*16的大小。

当ST1状态寄存器VMAP=0时， 0X000000-0X000040作为中断向量的存储空间。

Figure 2−11. Bit Fields of Status Register 1 (ST1)

15	13	12	11	10	9	8
ARP		XF	M0M1MAP	Reserved	OBJMODE	AMODE
R/W-000		R/W−0	R/W−1	R/W−0	R/W−0	R/W−0

7	6	5	4	3	2	1	0
IDLESTAT	EALLOW	LOOP	SPA	VMAP	PAGE0	DBGM	INTM
R−0	R/W−0	R−0	R/W−0	R/W−1	R/W−0	R/W−1	R/W−1

VMAP
Bit 3

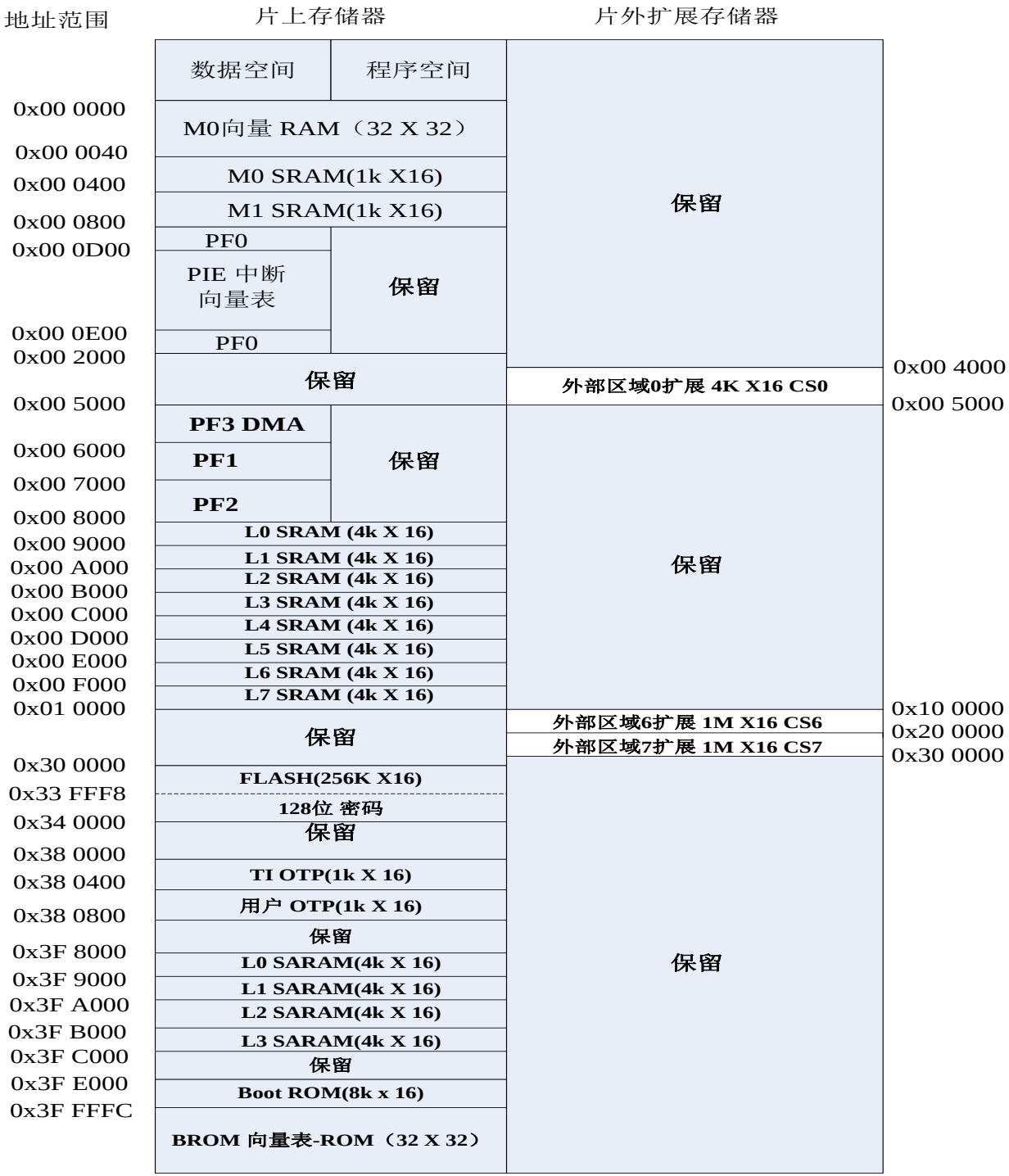
Vector map bit. VMAP determines whether the CPU interrupt vectors (including the reset vector) are mapped to the lowest or highest addresses in program memory:

0 CPU interrupt vectors are mapped to the bottom of program memory, addresses $00\ 0000_{16}$−$00\ 003F_{16}$.

1 CPU interrupt vectors are mapped to the top of program memory, addresses $3F\ FFC0_{16}$−$3F\ FFFF_{16}$.

On C28x designs, the VMAP signal is tied high internally, forcing the VMAP bit to be set high on a reset.

This bit can be individually set and cleared by the SETC VMAP instruction and CLRC VMAP instruction, respectively.



F26335的各存储器地址都是连续编码的，且空间地址是唯一的。

图5.1左半部分，首先对M0 SRAM从0X000000开始编码一直到0X000400结束，可以计算出这是1K*16的大小。

M1 SRAM从0X000400开始编码一直到0X000800结束，也是1K*16的大小。

接着是外设帧0、1、2、3，其中外设帧1、2、3还标注着Protected.

表 3-8. 外设帧 0 寄存器(1)

名称	地址范围	大小 (x 16)	访问类型(2)
器件仿真寄存器	0x00 0880-0x00 09FF	384	受 EALLOW 保护
闪存寄存器(3)	0x00 0A80-0x00 0ADF	96	受 EALLOW 保护
代码安全模块寄存器	0x00 0AE0-0x00 0AEF	16	受 EALLOW 保护
ADC 寄存器（双映射） 0 等待 (DMA)，1 个等待 (CPU)，只读	0x00 0B00-0x00 0B0F	16	不受 EALLOW 保护
XINTF 寄存器	0x00 0B20-0x00 0B3F	32	受 EALLOW 保护
CPU 定时器 0，CPU 定时器 1，CPU 定时器 2 寄存器	0x00 0C00-0x00 0C3F	64	不受 EALLOW 保护
PIE 寄存器	0x00 0CE0-0x00 0CFF	32	不受 EALLOW 保护
PIE 矢量表	0x00 0D00-0x00 0DFF	256	受 EALLOW 保护
DMA 寄存器	0x00 1000-0x00 11FF	512	受 EALLOW 保护

(1) 在帧 0 中的寄存器支持 16 位和 32 位访问。
(2) 如果寄存器是 EALLOW 受保护的，那么在 EALLOW 指令被执行前写入不能被执行。 EDIS 指令禁用写入以防止杂散代码或指针破坏寄存器内容。
(3) 闪存寄存器也受到代码安全模块 (CSM) 的保护。

表 **3-9.** 外设帧 **1** 寄存器

名称	地址范围	大小 **(x 16)**
eCAN-A 寄存器	0x00 6000-0x00 61FF	512
eCAN-B 寄存器	0x00 6200–0x00 63FF	512
ePWM1 + HRPWM1 寄存器	0x00 6800-0x00 683F	64
ePWM2 + HRPWM2 寄存器	0x00 6840-0x00 687F	64
ePWM3 + HRPWM3 寄存器	0x00 6880-0x00 68BF	64
ePWM4 + HRPWM4 寄存器	0x00 68C0-0x00 68FF	64
ePWM5 + HRPWM5 寄存器	0x00 6900-0x00 693F	64
ePWM6 + HRPWM6 寄存器	0x00 6940-0x00 697F	64
eCAP1 寄存器	0x00 6A00-0x00 6A1F	32
eCAP2 寄存器	0x00 6A20-0x00 6A3F	32
eCAP3 寄存器	6x40 6A00-0x00 0A5F	32
eCAP4 寄存器	6x60 6A00-0x00 0A7F	32
eCAP5 寄存器	6x80 6A00-0x00 0A9F	32
eCAP6 寄存器	0x00 6AA0–0x00 6ABF	32
eQEP1 寄存器	0x00 6B00-0x00 6B3F	64
eQEP2 寄存器	0x00 6B40-0x00 6B7F	64
GPIO 寄存器	0x00 6F80-0x00 6FFF	128

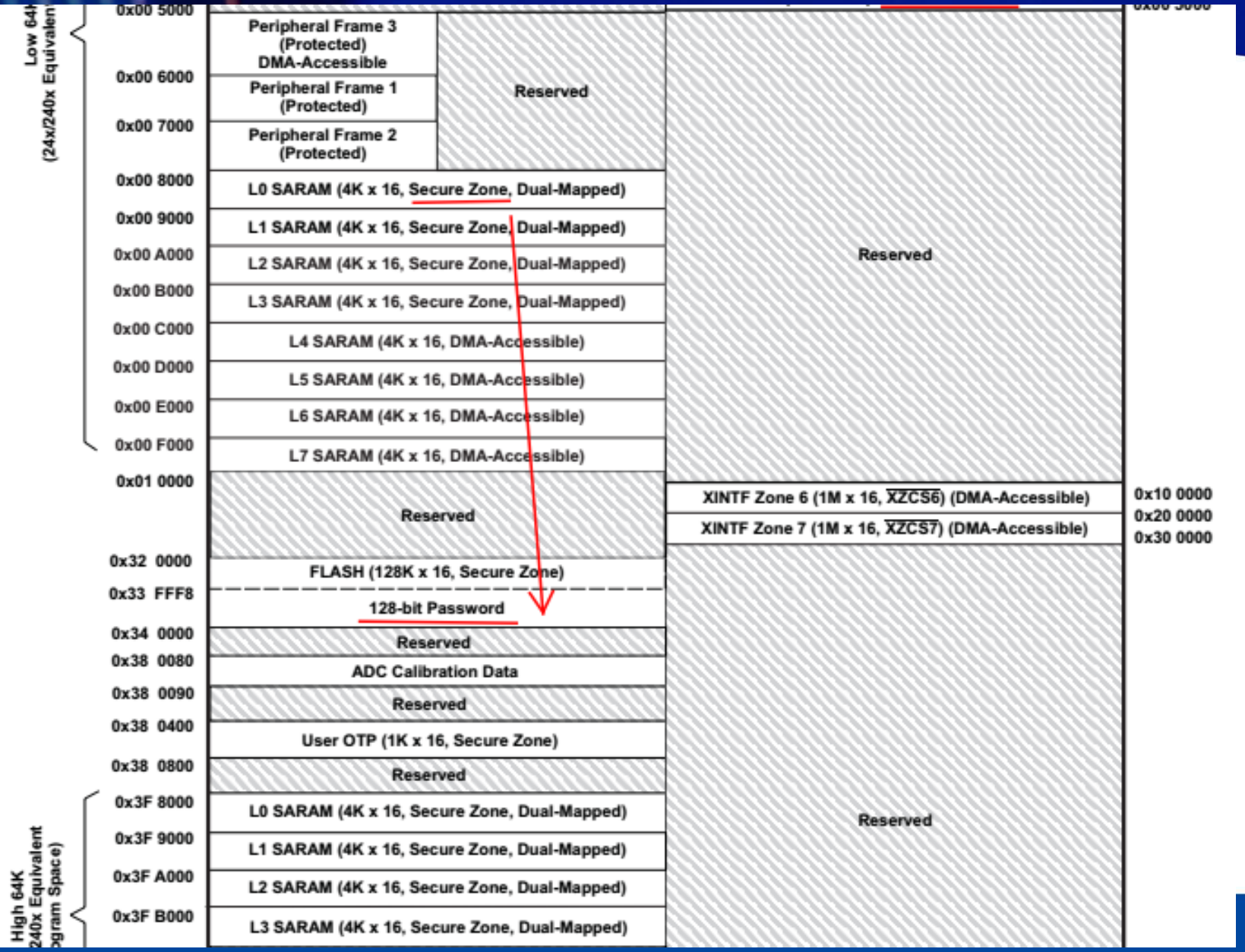
表 3-10. 外设帧 2 寄存器

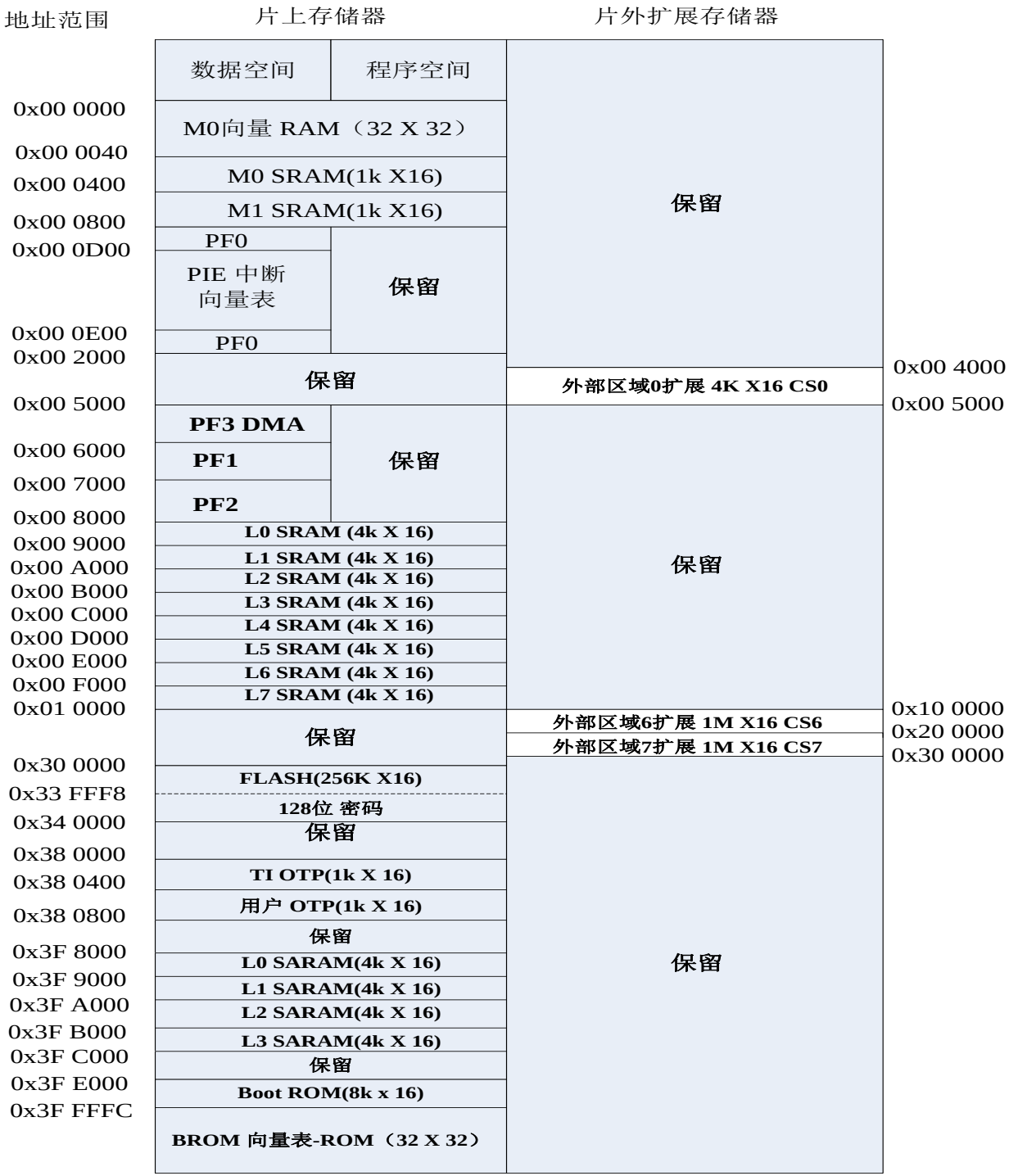
名称	地址范围	大小 (x 16)
系统控制寄存器	0x00 7010-0x00 702F	32
SPI-A 寄存器	0x00 7040-0x00 704F	16
SCI-A 寄存器	0x00 7050-0x00 705F	16
外部中断寄存器	0x00 7070-0x00 707F	16
ADC 寄存器	0x00 7100-0x00 711F	32
SCI-B 寄存器	0x00 7750-0x00 775F	16
SCI-C 寄存器	0x00 7770-0x00 777F	16
I2C-A 寄存器	0x00 7900-0x00 793F	64

表 3-11. 外设帧 3 寄存器

名称	地址范围	大小 (x 16)
McBSP-A 寄存器 (DMA)	0x5000 -0x503 F	64
McBSP-B 寄存器 (DMA)	0x5040 -0x507 F	64
ePWM1 + HRPWM1 (DMA)(1)	0x5800 -0x583 F	64
ePWM2 + HRPWM2 (DMA)	0x5840 -0x587 F	64
ePWM3 + HRPWM3 (DMA)	0x5880-0x58BF	64
ePWM4 + HRPWM4 (DMA)	0x58C0-0x58FF	64
ePWM5 + HRPWM5 (DMA)	0x5900 -0x593 F	64
ePWM6 + HRPWM6 (DMA)	0x5940 -0x597 F	64

(1) EPWM 和 HRPWM 模块可以被重新映射到可以被 DMA 模块访问的外设帧 3。 要做到这点，MAPCNF 寄存器（地址 0x702E）的位 0（MAPEPWM） 必须被设置为 1。此寄存器受 EALLOW 保护。 当此位为 0 时，ePWM 和 HRPWM 模块被映射到外设帧 1。


Low 64K (24x/240x Equivalent)
0x00 5000
Peripheral Frame 3 (Protected) DMA-Accessible
0x00 6000
Peripheral Frame 1 (Protected)
0x00 7000
Peripheral Frame 2 (Protected)
Reserved
0x00 8000
L0 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x00 9000
L1 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x00 A000
L2 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x00 B000
L3 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x00 C000
L4 SARAM (4K x 16, DMA-Accessible)
0x00 D000
L5 SARAM (4K x 16, DMA-Accessible)
0x00 E000
L6 SARAM (4K x 16, DMA-Accessible)
0x00 F000
L7 SARAM (4K x 16, DMA-Accessible)
0x01 0000
Reserved
Reserved
XINTF Zone 6 (1M x 16, XZCS6) (DMA-Accessible)
0x10 0000
XINTF Zone 7 (1M x 16, XZCS7) (DMA-Accessible)
0x20 0000
0x30 0000
0x32 0000
FLASH (128K x 16, Secure Zone)
0x33 FFF8
128-bit Password
0x34 0000
Reserved
0x38 0080
ADC Calibration Data
0x38 0090
Reserved
0x38 0400
User OTP (1K x 16, Secure Zone)
0x38 0800
Reserved
0x3F 8000
L0 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x3F 9000
L1 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x3F A000
L2 SARAM (4K x 16, Secure Zone, Dual-Mapped)
0x3F B000
L3 SARAM (4K x 16, Secure Zone, Dual-Mapped)
Reserved
High 64K (240x Equivalent ogram Space)



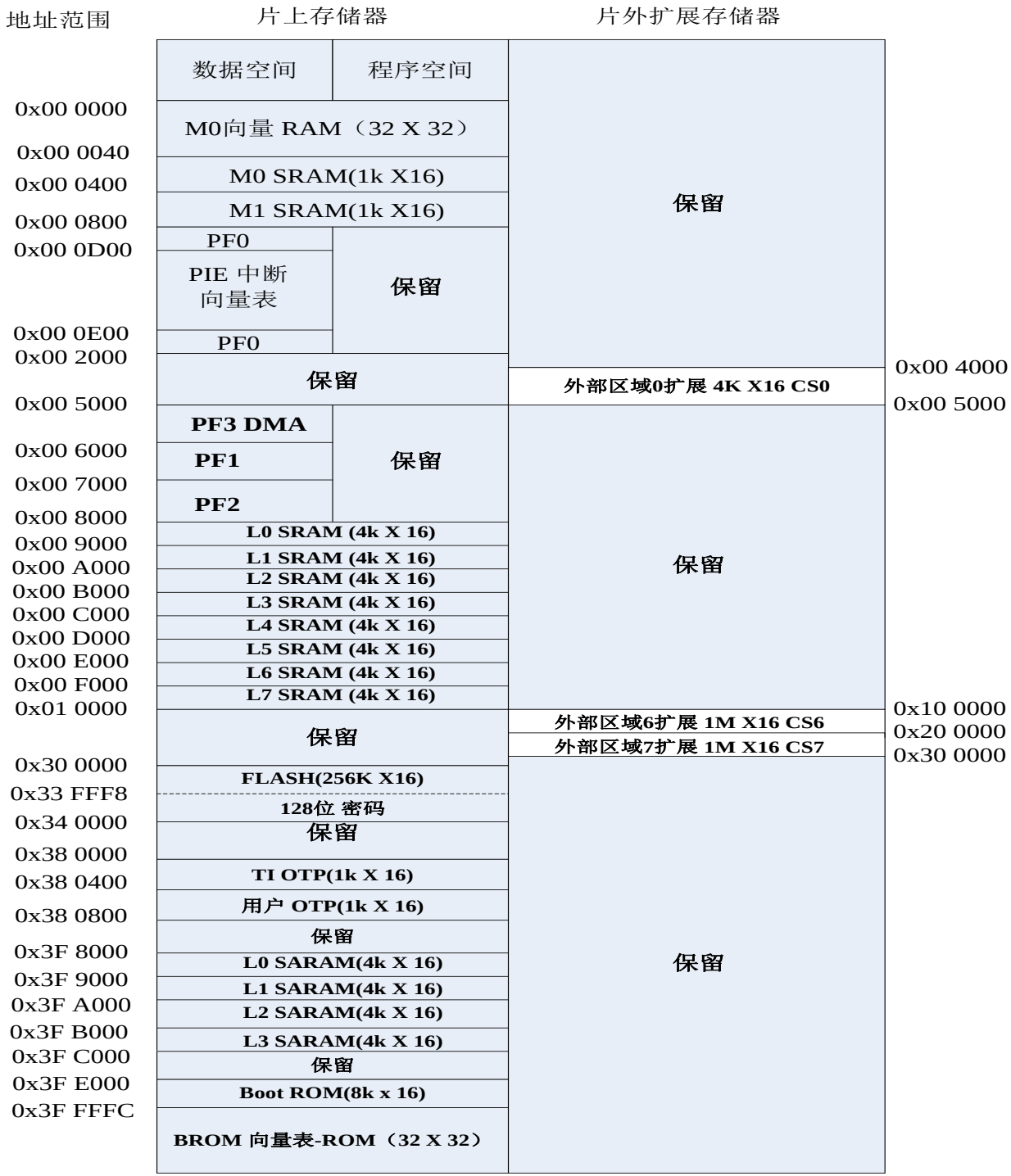
0X002000-0X005000是保留区，这段保留区被用作外部扩展区0，从这里也可以看出保留区的作用，这个外扩区同样是受保护的。外扩区还有分别为1M大小的6区与7区。

接下来是L0-L7的SRAM区，均为4K大小。下面是256K的FLASH空间。中间0X33FFF8-0X340000共128位用来保存CSM模块密码，保护FLASH、L0-L7、OTP空间内存放的数据。

下面是2K的OTP空间，其中1K OTP空间主要是TI用来测试的引导程序。

表 3-1. F28335，F28235 中闪存扇区的地址

地址范围	程序和数据空间
0x30 0000-0x30 7FFF	扇区 H (32K x 16)
0x30 8000-0x30 FFFF	扇区 G (32K x 16)
0x31 0000-0x31 7FFF	扇区 F (32K x 16)
0x31 8000-0x31 FFFF	扇区 E (32K x 16)
0x32 0000-0x32 7FFF	扇区 D (32K x 16)
0x32 8000-0x32 FFFF	扇区 C (32K x 16)
0x33 0000-0x33 7FFF	扇区 B (32K x 16)
0x33 8000-0x33 FF7F	扇区 A (32K x 16)
0x33 FF80-0x33 FFF5	当使用 代码安全模块时，编程至 0x0000
0x33 FFF6-0x33 FFF7	引导至闪存进入点 （程序分支指令所在的位置）
0x33 FFF8-0x33 FFFF	安全密码 （128 位）（不要设定为全零）



接下来是L0-L3 SARAM空间，这是个双映射空间，也就是名字是一样的，但空间地址是不一样的，这样有利于数据备份。

接下来是8K的BOOT ROM空间，用来存放Boot loader程序，系统初始引导程序。

表 3-6. 引导模式选择

模式	GPIO87/XA15	GPIO86/XA14	GPIO85/XA13	GPIO84/XA12	模式(1)
F	1	1	1	1	跳转到闪存
E	1	1	1	0	SCI-A boot
D	1	1	0	1	SPI-A 引导
C	1	1	0	0	I2C-A 引导
B	1	0	1	1	eCAN-A 引导
A	1	0	1	0	McBSP-A 引导
9	1	0	0	1	跳转到 XINTF x16
8	1	0	0	0	跳转到 XINTF x32
7	0	1	1	1	跳转到 OTP
6	0	1	1	0	并行 GPIO I/O 引导
5	0	1	0	1	并行 XINTF 引导
4	0	1	0	0	跳转至 SARAM
3	0	0	1	1	分支到检查引导模式
2	0	0	1	0	跳转到闪存, 跳过 ADC 校准
1	0	0	0	1	跳转至 SARAM, 跳过 ADC 校准
0	0	0	0	0	跳转至 SCI, 跳过 ADC 校准

(1) 所有的 4 个 GPIO 引脚都有内部上拉电阻器。

在上电过程中对于F28335处理器有16种不同的启动模式，可以通过处理器的GPIO84-87 4个端口控制，如表16.2。

TMS320F28335存储器的特点

1.片上SRAM

SRAM即单口随机读/写存储器，有别于双口RAM，双口RAM是在一个SRAM存储器上具有两套完全独立的数据线、地址线和读写控制线，并允许两个独立的系统同时对该存储器进行随机性访问。

F28335片内共有34K*16位单周期单次访问随机存储器SRAM，被分成10块，分别为M0、M1、L0-L7。

M0和M1块SRAM的大小均为1K*16位，当复位后，堆栈指针指向M1块的起始地址，堆栈指针向上生长。 M0和M1段都可以映射到程序区和数据区。

TMS320F28335存储器的特点

1.片上SRAM

L0-L7块SRAM的大小均为4K*16位，既可映射到程序空间，也可映射到数据空间，其中L0-L3复制可映射到两块不同的地址空间并且受片上的FLASH中的密码保护，以免存在上面的程序或数据，被他人非法。

TMS320F28335存储器的特点

2. BOOT ROM

BOOT ROM ，可以叫做引导ROM，主要装载了TI的引导装载程序，实现DSP的Boot loader功能。MP/MC=0时，DSP被设置为微计算机模式，CPU在复位后，指令跳转到0X3FFC00-0X3FFFBF区间内，执行Boot loader程序，在后续F28335的引导程序章节（16章）中会进一步介绍系统是如何引导的。

TMS320F28335存储器的特点

3. 片上FLASH和OTP

F28335片上有256K*16位嵌入式FLASH 存储器2K*16位一次可编程OTP存储器，它们均受片上FLASH中的密码保护。FLASH存储器由8个32K *16位扇区组成，用户可以对其中任何一个扇区进行擦除、编程和校验，而其它扇区不变。但是，不能在其中一个扇区上执行程序来擦除和编程其它的扇区。其主要有一下特点：

- 整个存储器分成多段
- 代码安全保护
- 低功耗模式
- 可根据CPU频率调整等待周期
- FLASH流水线模式能够提高线性代码的执行效率

TMS320F28335存储器的特点

3. 片上FLASH和OTP

F28335片内FLASH存储器的分段情况见表5.1。

28335的OTP存储器也是统一映射到程序和数据存储器空间，既可以为数据存储器也可以为程序存储器，与FLASH存储器不同的是它只能被用户写一次，態再次被擦除。

FLASH和OTP存储器的功耗模式有以下3种：

① 重启或睡眠状态

② 备用状态

③ 激活状态

TMS320F28335存储器的特点

3. 片上FLASH和OTP

FLASH和OTP存储器的功耗模式有以下3种：

1）重启或睡眠状态

芯片复位后，FLASH 与OTP处于睡眠状态，CPU在FLASH和OTP存储器映射区域读数据或取代码使得状态改变，从睡眠状态变为备用状态，进一步会变为激活状态。

2）备用状态

该状态的功耗比睡眠状态大，需要较短的时间就转变为激活状态或读状态。

以上两个状态转换过程中，CPU自动延迟等待，一旦状态转换完成，CPU的访问恢复正常。

TMS320F28335存储器的特点

3. 片上FLASH和OTP

FLASH和OTP存储器的功耗模式有以下3种：

3）在激活状态下，CPU在FLASH与OTP的存储器映射空间内读取访问受到FBANKWAIT寄存器和FOTPWAIT寄存器控制。

在状态转换时，从低功耗模式转换到高功耗模式，延时是必要的，通过延时可以使FLASH能够处在稳定的激活状态。在延时期间，CPU都会自动等待直到延时完成为止。

睡眠到备用受FSTDBWAIT控制，备用到激活受FACTIVEWAIT寄存器控制。

Figure 1. Flash Power Mode State Diagram

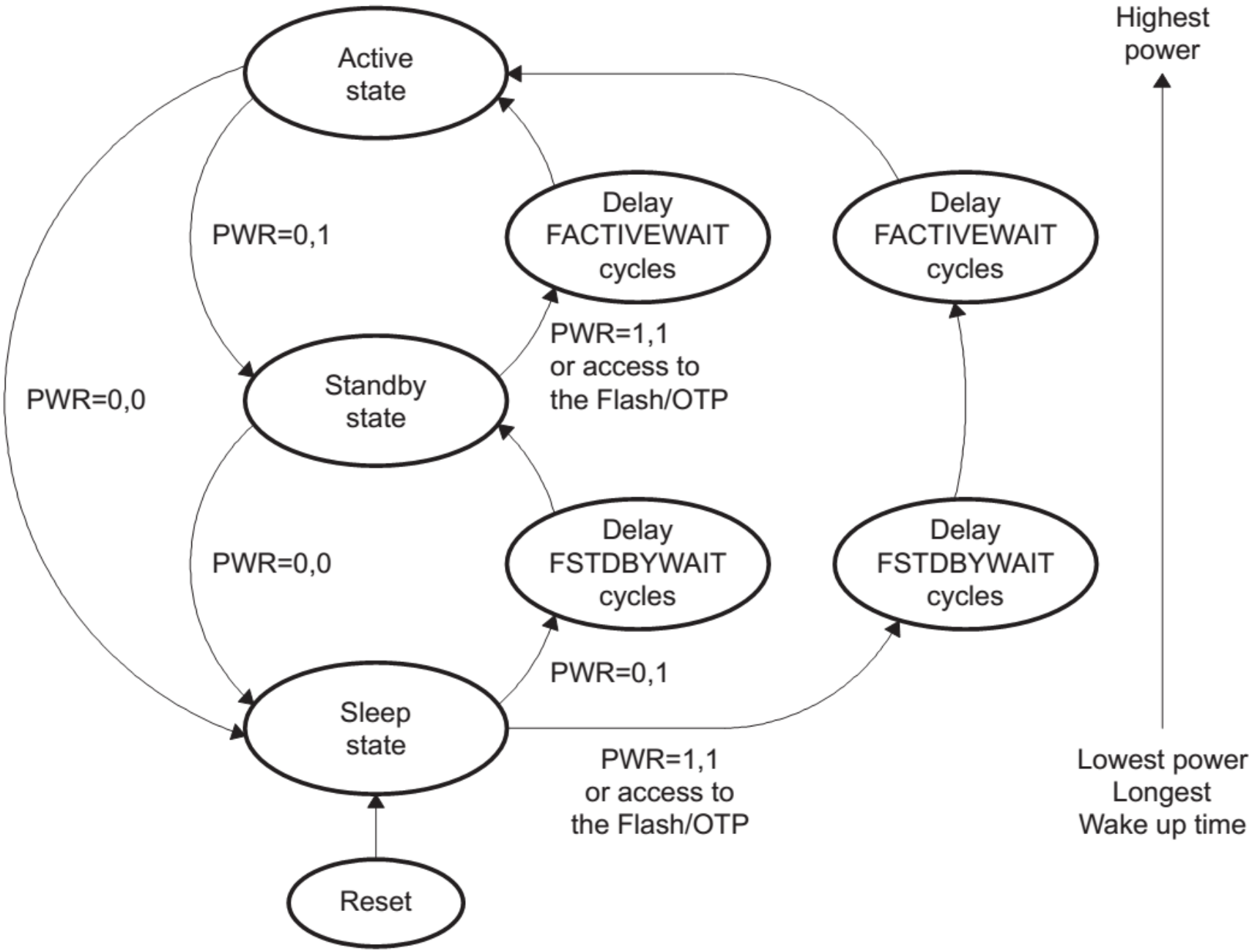


Figure 5. Flash Power Register (FPWR)

15	2	1	0
Reserved		PWR	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

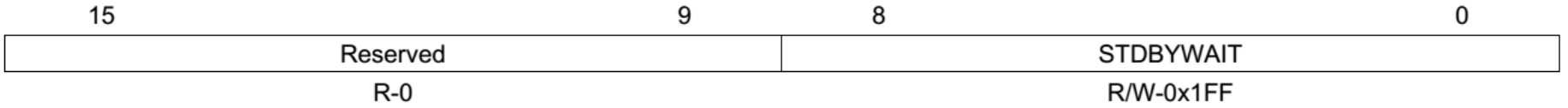
Table 3. Flash Power Register (FPWR) Field Descriptions

Bit	Field	Value	Description (1) (2)
15-2	Reserved		
1-0	PWR		Flash Power Mode Bits. Writing to these bits changes the current power mode of the flash bank and pump. See section Section 2 for more information on changing the flash bank power mode.
		00	Pump and bank sleep (lowest power)
		01	Pump and bank standby
		10	Reserved (no effect)
		11	Pump and bank active (highest power)

(1) This register is EALLOW protected. See Section 7.2 for more information.

(2) This register is protected by the Code Security Module (CSM). See Section 4 for more information.

Figure 7. Flash Standby Wait Register (FSTDBYWAIT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

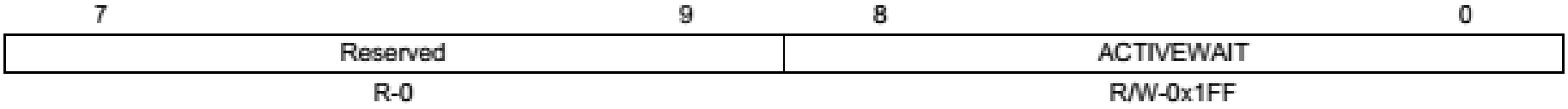
Table 5. Flash Standby Wait Register (FSTDBYWAIT) Field Descriptions

Bit	Field	Value	Description [1] [2]
15-9	Reserved	0	Reserved
8-0	STDBYWAIT		**This register should be left in its default state.**
			Bank and Pump Sleep To Standby Wait Count.
		111111111	511 SYSCLKOUT cycles (default)

(1) This register is EALLOW protected. See Section 7.2 for more information.

(2) This register is protected by the Code Security Module (CSM). See Section 4 for more information.

Figure 8. Flash Standby to Active Wait Counter Register (FACTIVEWAIT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 6. Flash Standby to Active Wait Counter Register (FACTIVEWAIT) Field Descriptions

Bits	Field	Value	Description [1] [2]
15-9	Reserved	0	Reserved
8-0	ACTIVEWAIT		**This register should be left in its default state.**
			Bank and Pump Standby To Active Wait Count:
		111111111	511 SYSCLKOUT cycles (default)

(1) This register is EALLOW protected. See Section 7.2 for more information.

(2) This register is protected by the Code Security Module (CSM). See Section 4 for more information.

Figure 9. Flash Wait-State Register (FBANKWAIT)

15 12	11 8	7 4	3 0
Reserved	PAGEWAIT	Reserved	RANDWAIT
R-0	R/W-0xF	R-0	R/W-0xF

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. Flash Wait-State Register (FBANKWAIT) Field Descriptions

Bits	Field	Value	Description (1) (2) (3)
15-12	Reserved		Reserved
11-8	PAGEWAIT		Flash Paged Read Wait States. These register bits specify the number of wait states for a paged read operation in CPU clock cycles (0..15 SYSCLKOUT cycles) to the flash bank. See Section 2.1 for more information. See the device-specific data manual for the minimum time required for a PAGED flash access. You must set RANDWAIT to a value greater than or equal to the PAGEWAIT setting. No hardware is provided to detect a PAGEWAIT value that is greater then RANDWAIT.
		0000	Illegal value. PAGEWAIT must be set greater then 0.
		0001	One wait state per paged flash access or a total of two SYSCLKOUT cycles per access.
		0010	Two wait states per paged flash access or a total of three SYSCLKOUT cycles per access.
		0011	Three wait states per paged flash access or a total of four SYSCLKOUT cycles per access.
		. . .	. . .
		1111	15 wait states per paged flash access or a total of 16 SYSCLKOUT cycles per access. (default)
7-4	Reserved		Reserved
3-0	RANDWAIT		Flash Random Read Wait States. These register bits specify the number of wait states for a random read operation in CPU clock cycles (1..15 SYSCLKOUT cycles) to the flash bank. See Section 2.1 for more information. See the device-specific data manual for the minimum time required for a RANDOM flash access. RANDWAIT must be set greater than 0. That is, at least 1 random wait state must be used. In addition, you must set RANDWAIT to a value greater than or equal to the PAGEWAIT setting. The device will not detect and correct a PAGEWAIT value that is greater then RANDWAIT.
		0000	Illegal value. RANDWAIT must be set greater then 0.
		0001	One wait state per random flash access or a total of two SYSCLKOUT cycles per access.
		0010	Two wait states per random flash access or a total of three SYSCLKOUT cycles per access.
		0011	Three wait states per random flash access or a total of four SYSCLKOUT cycles per access.
		. . .	. . .
		1111	15 wait states per random flash access or a total of 16 SYSCLKOUT cycles per access. (default)

Figure 10. OTP Wait-State Register (FOTPWAIT)

15	5	4	0
Reserved		OTPWAIT	
R-0		R/W-0x1F	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. OTP Wait-State Register (FOTPWAIT) Field Descriptions

Bit(s)	Field	Value	Description [1] [2] [3]
15-5	Reserved	0	Reserved
4-0	OTPWAIT		OTP Read Wait States. These register bits specify the number of wait states for a read operation in CPU clock cycles (1..31 SYSCLKOUT cycles) to the OTP. See CPU Read Or Fetch Access From flash/OTP section for details. There is no PAGE mode in the OTP. OTPWAIT must be set greater than 0. That is, a minimum of 1 wait state must be used. See the device-specific data manual for the minimum time required for an OTP access.
		00000	Illegal value. OTPWAIT must be set to 1 or greater.
		00001	One wait state will be used each OTP access for a total of two SYSCLKOUT cycles per access.
		00010	Two wait states will be used for each OTP access for a total of three SYSCLKOUT cycles per access.
		00011	Three wait states will be used for each OTP access for a total of four SYSCLKOUT cycles per access.
		. . .	. . .
		11111	31 wait states will be used for an OTP access for a total of 32 SYSCLKOUT cycles per access.

(1) This register is EALLOW protected. See Section 7.2 for more information.
(2) This register is protected by the Code Security Module (CSM). See Section 4 for more information.
(3) When writing to this register, follow the procedure described in Section 2.4.

TMS320F28335存储器的特点

对FLASH和OTP存储器来说，CPU读写数据操作主要有以下3种形式：

1.32位取指令

2.16位或32位数据空间读操作

3.16位程序空间读操作

一旦FLASH处于激活状态，那么对存储器映射区的访问可以被分为FLASH访问或OTP访问，OTP存储器小于4M，在22位取地址范围内，FLASH则大于4M，所以FLASH访问时，又分为存储器的随机访问与存储器的页访问。

FLASH存储器时一阵列形式组成，每行又2048位，首次访问的某一行称为随机访问，若随后又访问该行则称为页访问，一个随机和页访问的等待状态数可通过FBANKWAIT寄存器编程配置。

Figure 9. Flash Wait-State Register (FBANKWAIT)

15 12	11 8	7 4	3 0
Reserved	PAGEWAIT	Reserved	RANDWAIT
R-0	R/W-0xF	R-0	R/W-0xF

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 7. Flash Wait-State Register (FBANKWAIT) Field Descriptions

Bits	Field	Value	Description (1) (2) (3)
15-12	Reserved		Reserved
11-8	PAGEWAIT		Flash Paged Read Wait States. These register bits specify the number of wait states for a paged read operation in CPU clock cycles (0..15 SYSCLKOUT cycles) to the flash bank. See Section 2.1 for more information. See the device-specific data manual for the minimum time required for a PAGED flash access. You must set RANDWAIT to a value greater than or equal to the PAGEWAIT setting. No hardware is provided to detect a PAGEWAIT value that is greater then RANDWAIT.
		0000	Illegal value. PAGEWAIT must be set greater then 0.
		0001	One wait state per paged flash access or a total of two SYSCLKOUT cycles per access.
		0010	Two wait states per paged flash access or a total of three SYSCLKOUT cycles per access.
		0011	Three wait states per paged flash access or a total of four SYSCLKOUT cycles per access.
		. . .	. . .
		1111	15 wait states per paged flash access or a total of 16 SYSCLKOUT cycles per access. (default)
7-4	Reserved		Reserved
3-0	RANDWAIT		Flash Random Read Wait States. These register bits specify the number of wait states for a random read operation in CPU clock cycles (1..15 SYSCLKOUT cycles) to the flash bank. See Section 2.1 for more information. See the device-specific data manual for the minimum time required for a RANDOM flash access. RANDWAIT must be set greater than 0. That is, at least 1 random wait state must be used. In addition, you must set RANDWAIT to a value greater than or equal to the PAGEWAIT setting. The device will not detect and correct a PAGEWAIT value that is greater then RANDWAIT.
		0000	Illegal value. RANDWAIT must be set greater then 0.
		0001	One wait state per random flash access or a total of two SYSCLKOUT cycles per access.
		0010	Two wait states per random flash access or a total of three SYSCLKOUT cycles per access.
		0011	Three wait states per random flash access or a total of four SYSCLKOUT cycles per access.
		. . .	. . .
		1111	15 wait states per random flash access or a total of 16 SYSCLKOUT cycles per access. (default)

TMS320F28335存储器的特点

OTP存储器的访问速度通常可以通过FOTPWAIT 中的OTPWAIT位来控制。OTP存储器的访问时间比FLASH要长。

FLASH的流水线模式：FLASH存储器数据掉电不丢失，所以通常用来保护代码。在代码执行期间，除非有中断发生，指令可从存储器地址中连续获取，连续地址中的部分代码组成了主要的代码，称为线性代码。为了提高线性代码的执行性能，可采用FLASH流水线模式，且FLASH流水线模式独立于CPU的流水线模式。

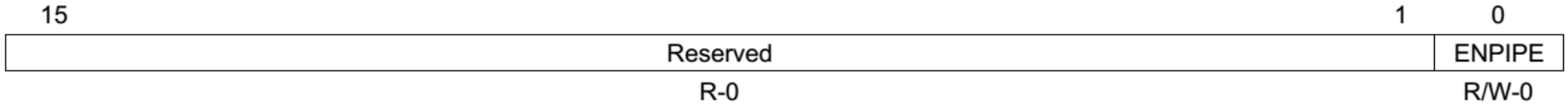
FLASH 或OTP存储器的相关配置寄存器见表5.2。

Table 1. Flash/OTP Configuration Registers

Name [1] [2]	Address	Size (x16)	Description	Bit Description
FOPT	0x0A80	1	Flash Option Register	Figure 4
Reserved	0x0A81	1	Reserved	
FPWR	0x0A82	1	Flash Power Modes Register	Figure 5
FSTATUS	0x0A83	1	Status Register	Figure 6
FSTDBYWAIT [3]	0x0A84	1	Flash Sleep To Standby Wait Register	Figure 7
FACTIVEWAIT [3]	0x0A85	1	Flash Standby To Active Wait Register	Figure 8
FBANKWAIT	0x0A86	1	Flash Read Access Wait State Register	Figure 9
FOTPWAIT	0x0A87	1	OTP Read Access Wait State Register	Figure 10

(1) These registers are EALLOW protected. See Section 7.2 for information.
(2) These registers are protected by the Code Security Module (CSM). See Section 4 for more information.
(3) These registers should be left in their default state.

Figure 4. Flash Options Register (FOPT)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2. Flash Options Register (FOPT) Field Descriptions

Bit	Field	Value	Description (1) (2) (3)
15-1	Reserved		
0	ENPIPE		Enable Flash Pipeline Mode Bit. Flash pipeline mode is active when this bit is set. The pipeline mode improves performance of instruction fetches by pre-fetching instructions. See Section 2.2 for more information. When pipeline mode is enabled, the flash wait states (paged and random) must be greater than zero. On flash devices, ENPIPE affects fetches from flash and OTP.
		0	Flash Pipeline mode is not active. (default)
		1	Flash Pipeline mode is active.

(1) This register is EALLOW protected. See Section 7.2 for more information.

(2) This register is protected by the Code Security Module (CSM). See Section 4 for more information.

(3) When writing to this register, follow the procedure described in Section 2.4.

第五讲：存储器以及地址分配

1、TMS320F28335存储器空间分配

2、TMS320F28335存储器保护特点

3、XINTF接口

4、相关寄存器介绍

TMS320F28335内存保护特点

代码安全模块CSM--代码安全模块（CSM）是F28335上程序安全性的主要手段，它禁止未授权的用户访问片内存储器，禁止私有代码的复制或者逆向操作。

安全模块限制CPU去访问片内存储器。实际上，对各种存储器的读写访问都是通过JTAG端口或外设来进行的，而CSM模块所谓的代码安全性主要是针对片内存储器的访问来定义的，用来禁止未经授权去复制私人代码或数据。

通过一个128位的密码（相当于8个16位的字）来对安全区来进行加密或解密。这段密码保存在FLASH的最后8个字中（0X33FFF8~0X33FFFF），也就是密码区中（PWL），通过密码匹配（PMF），可以解锁器件。

TMS320F28335内存保护特点

如果密码保护区中的128位数都是同一个数，这个器件不受保护。

全是同一个数有两种可能：一种全为0，另一种全为1。

一个新的FLASH或FLASH被擦除后，就变为全1了，这样只要读一下密码区，就能破解了；还一种情况，就是全为0，这时候器件是被加密了，但是不管密钥寄存器的内容是什么，器件都处在加密状态，即该器件无法解锁了，这时候芯片就被完全锁住了。

因此不要用全0作为密码。如果在擦除FLASH的期间，芯片复位了，那这个芯片的密码就不确定了，也不能解锁。

芯片不能解锁（用全零作为密码、FLASH擦除期间复位、忘记密码），这时芯片句完全锁住了，只能调试，不能重新烧写程序。

TMS320F28335内存保护特点

用户用来解锁的寄存器为密钥寄存器，在存储空间映射地址为0x0000 0AE0~0x0000 0AE7,该区域受EALLOW保护。

当这个128位的密钥位全1时，密钥寄存器不需要与之匹配。当一开始调试FLASH区加密的芯片的时候，仿真器取得CPU的控制权需要一定的时间，在此期间，CPU正在开始运行，并且会执行保护加密区的操作，这个操作会引起仿真器断开连接，有两个方法可以解决这个问题。

TMS320F28335内存保护特点

1、采用Wait-in-Reset仿真模式，这种方法是让芯片保持在复位状态直到仿真器得到控制，这种方法要求仿真器要能支持这种模式。

2、采用“Branch to check boot mode”引导。这个方法会持续不停的让引导模式选择引脚。可以选择这种引导模式，一旦仿真器通过重新映射PC到另外的地址或者改变引导模式选择引脚以进入引导而进行连接。

表 3-6. 引导模式选择

模式	GPIO87/XA15	GPIO86/XA14	GPIO85/XA13	GPIO84/XA12	模式(1)
F	1	1	1	1	跳转到闪存
E	1	1	1	0	SCI-A boot
D	1	1	0	1	SPI-A 引导
C	1	1	0	0	I2C-A 引导
B	1	0	1	1	eCAN-A 引导
A	1	0	1	0	McBSP-A 引导
9	1	0	0	1	跳转到 XINTF x16
8	1	0	0	0	跳转到 XINTF x32
7	0	1	1	1	跳转到 OTP
6	0	1	1	0	并行 GPIO I/O 引导
5	0	1	0	1	并行 XINTF 引导
4	0	1	0	0	跳转至 SARAM
3	0	0	1	1	分支到检查引导模式
2	0	0	1	0	跳转到闪存, 跳过 ADC 校准
1	0	0	0	1	跳转至 SARAM, 跳过 ADC 校准
0	0	0	0	0	跳转至 SCI, 跳过 ADC 校准

(1) 所有的 4 个 GPIO 引脚都有内部上拉电阻器。

在上电过程中对于F28335处理器有16种不同的启动模式，可以通过处理器的GPIO84-87 4个端口控制，如表16.2。

TMS320F28335内存保护特点

密码匹配流程：

对芯片解密的过程被称为密码匹配流程（PMF）。图5.2描述了该操作流程。PMF本质上是一个PWL中进行8次哑读，并对KEY寄存器进行8次写的过程。

PMF在进行解除DSP的安全性操作时可能遇到2种情况：

情况1：如果DSP在PWL处有密码，需要进行一下步骤：

① 从PWL处进行8次哑读

② 写密码到KEY寄存器

③ 如果密码正确，DSP就解锁；否则DSP仍被锁着

TMS320F28335内存保护特点

密码匹配流程：

情况2：如果DSP没有密码保护，那么PWL处应该全为1，需要进行以下步骤：

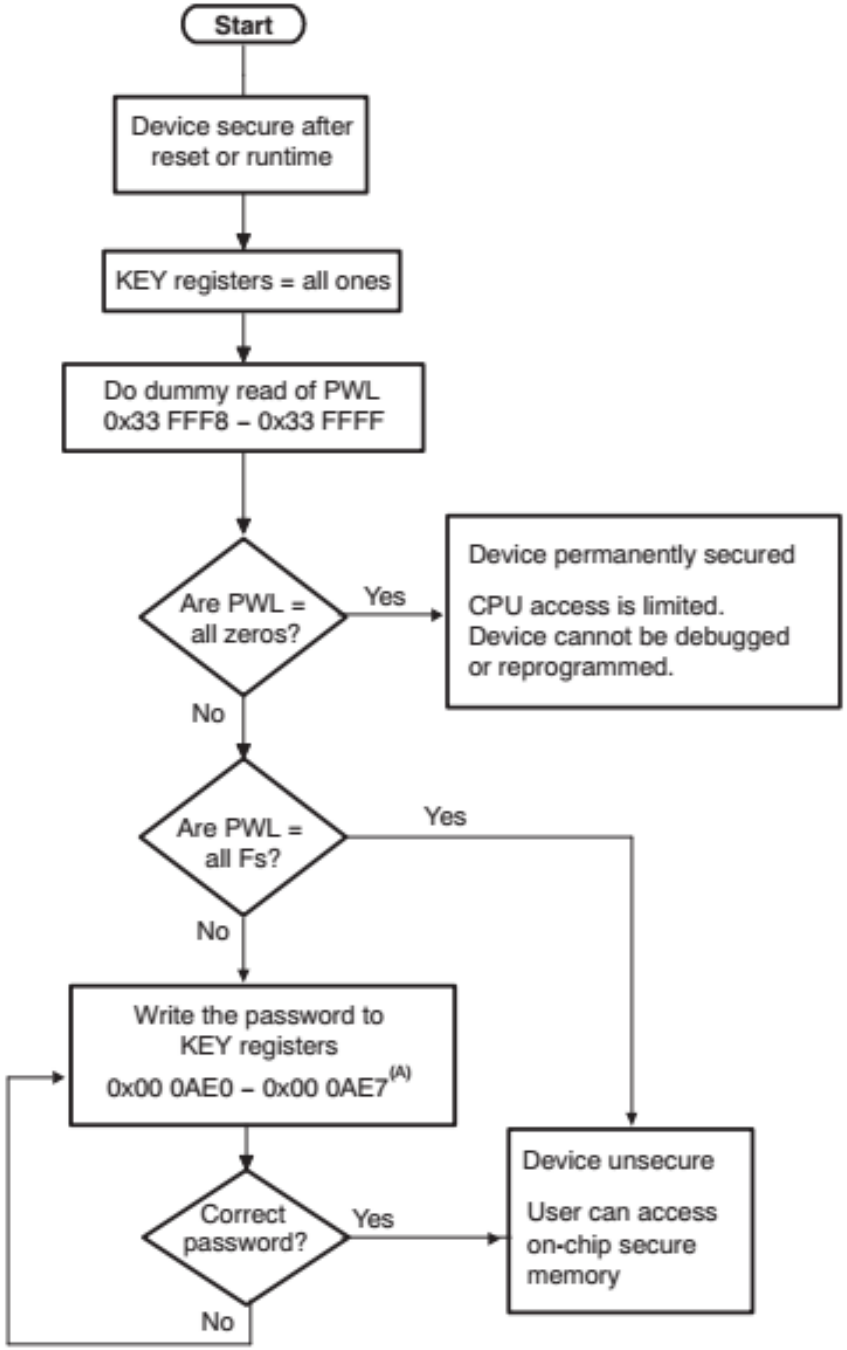
① 从PWL处进行哑读

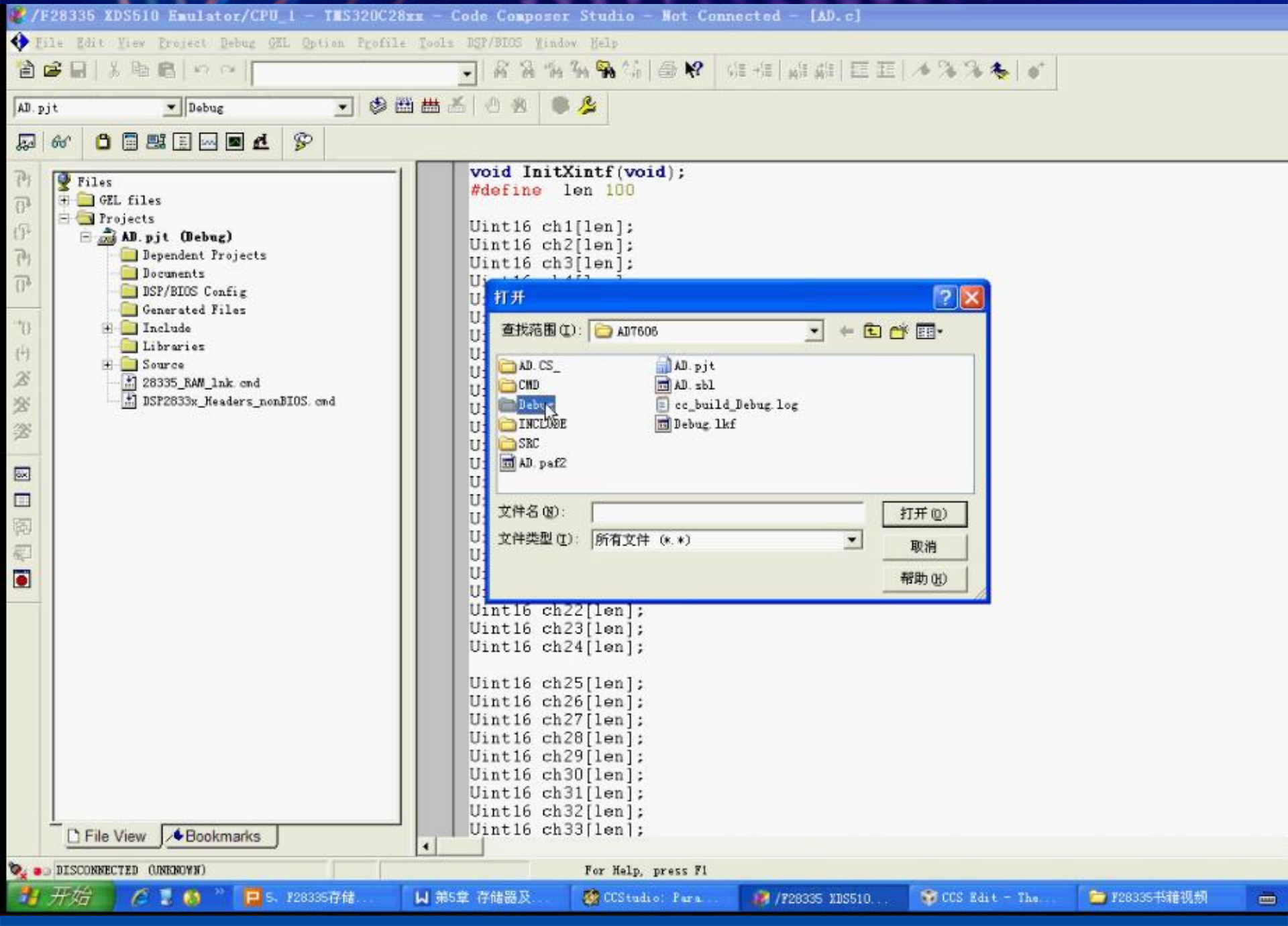
② 上面的操作完成后，DSP立马就解锁；可以随意对存储器进行操作

哑读：PWL中的内容实际上是不能读出的，执行读操作后读出的数据与PWL中真正的内容并不一致（全1和全0除外）。

具体程序见课本实例。

Figure 12. Password Match Flow (PMF)

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File Edit View Project Debug GEL Option Profile Tools DSP/BIOS Window Help
AD.pjt
Debug
Files
GEL files
Projects
AD.pjt (Debug)
Dependent Projects
Documents
DSP/BIOS Config
Generated Files
Include
Libraries
Source
28335_RAM_lnk.cmd
DSP2833x_Headers_nonBIOS.cmd
File View
Bookmarks
void InitXintf(void);
#define len 100
Uint16 ch1[len];
Uint16 ch2[len];
Uint16 ch3[len];
打开
查找范围(I):
AD7606
AD.CS_
CMD
Debug
INCLUDE
SRC
AD.paf2
AD.pjt
AD.sbl
cc_build_Debug.log
Debug.lkf
文件名(N):
文件类型(T):
所有文件 (*.*)
打开(O)
取消
帮助(H)
Uint16 ch22[len];
Uint16 ch23[len];
Uint16 ch24[len];
Uint16 ch25[len];
Uint16 ch26[len];
Uint16 ch27[len];
Uint16 ch28[len];
Uint16 ch29[len];
Uint16 ch30[len];
Uint16 ch31[len];
Uint16 ch32[len];
Uint16 ch33[len];
DISCONNECTED (UNKNOWN)
For Help, press F1
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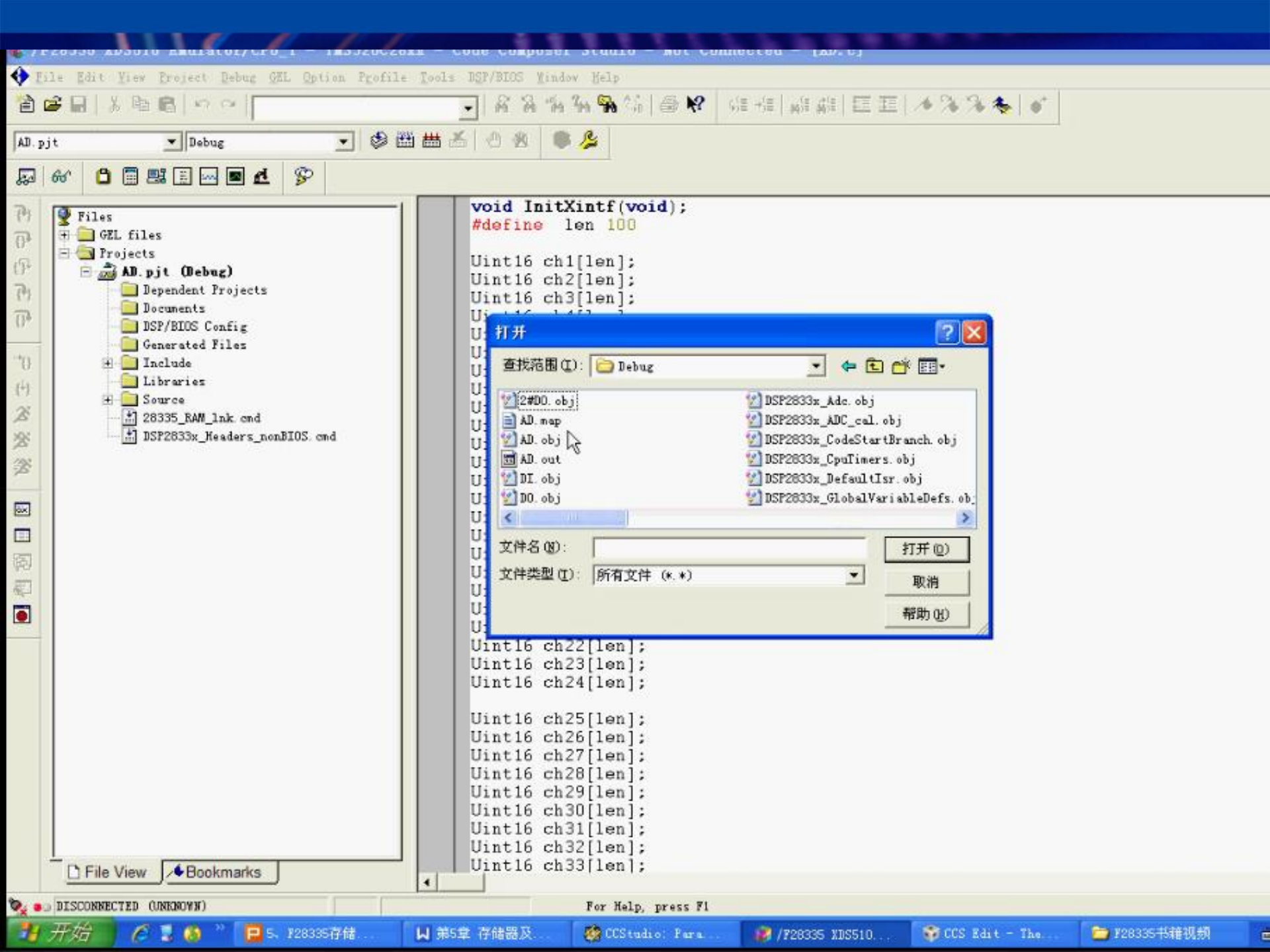
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28335_RAM_lnk.cmd
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File View
Bookmarks
void InitXintf(void);
#define len 100
Uint16 ch1[len];
Uint16 ch2[len];
Uint16 ch3[len];
打开
查找范围(I):
Debug
2#DO.obj
AD.map
AD.obj
AD.out
DI.obj
DO.obj
DSP2833x_Adc.obj
DSP2833x_ADC_cal.obj
DSP2833x_CodeStartBranch.obj
DSP2833x_CpuTimers.obj
DSP2833x_DefaultIsr.obj
DSP2833x_GlobalVariableDefs.ob
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文件类型(T):
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打开(O)
取消
帮助(H)
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Uint16 ch24[len];
Uint16 ch25[len];
Uint16 ch26[len];
Uint16 ch27[len];
Uint16 ch28[len];
Uint16 ch29[len];
Uint16 ch30[len];
Uint16 ch31[len];
Uint16 ch32[len];
Uint16 ch33[len];
DISCONNECTED (UNKNOWN)
For Help, press F1
开始
5、F28335存储...
第5章 存储器及...
CCStudio: Para...
/F28335 XDS510...
CCS Edit - The...
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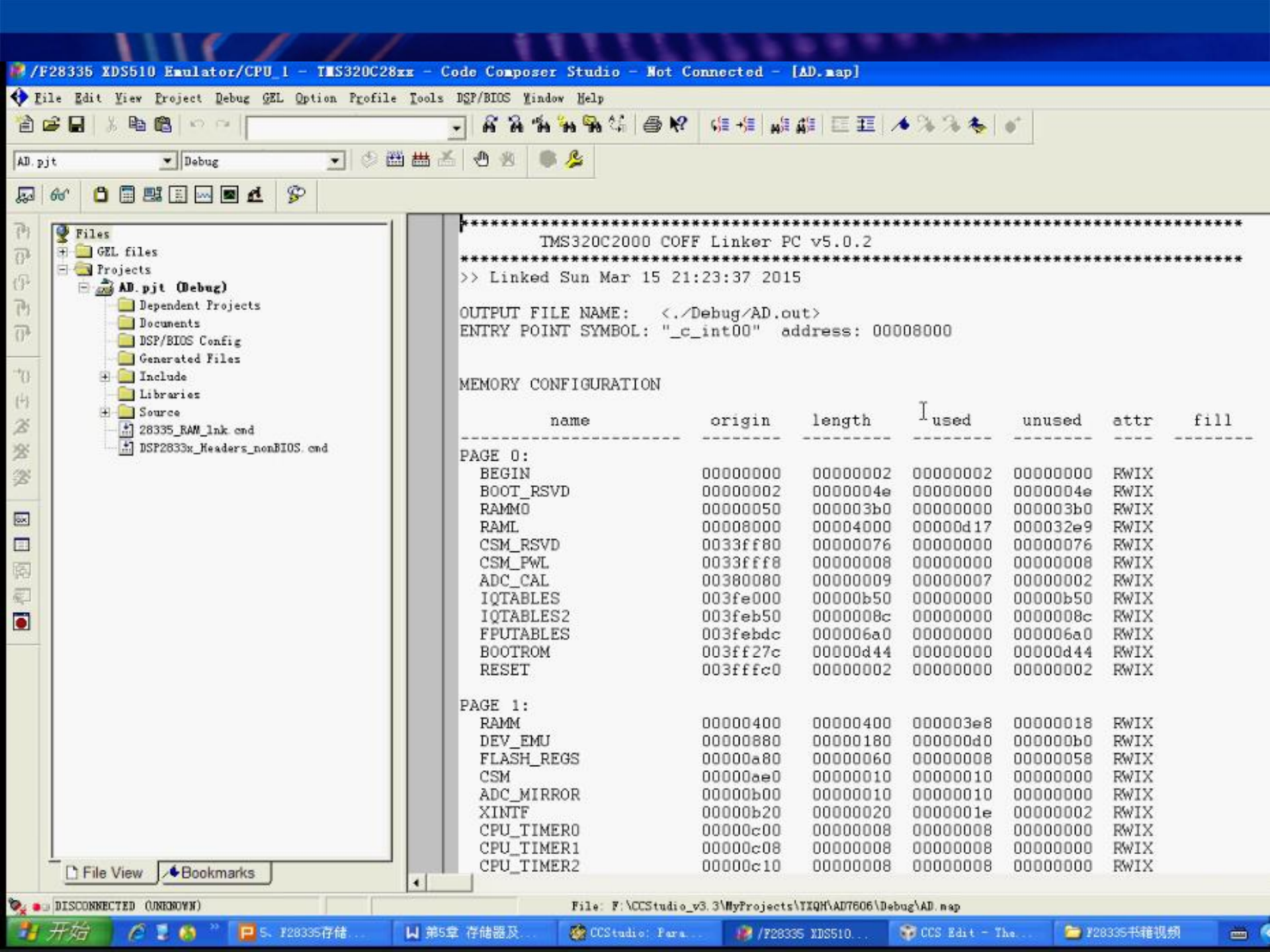
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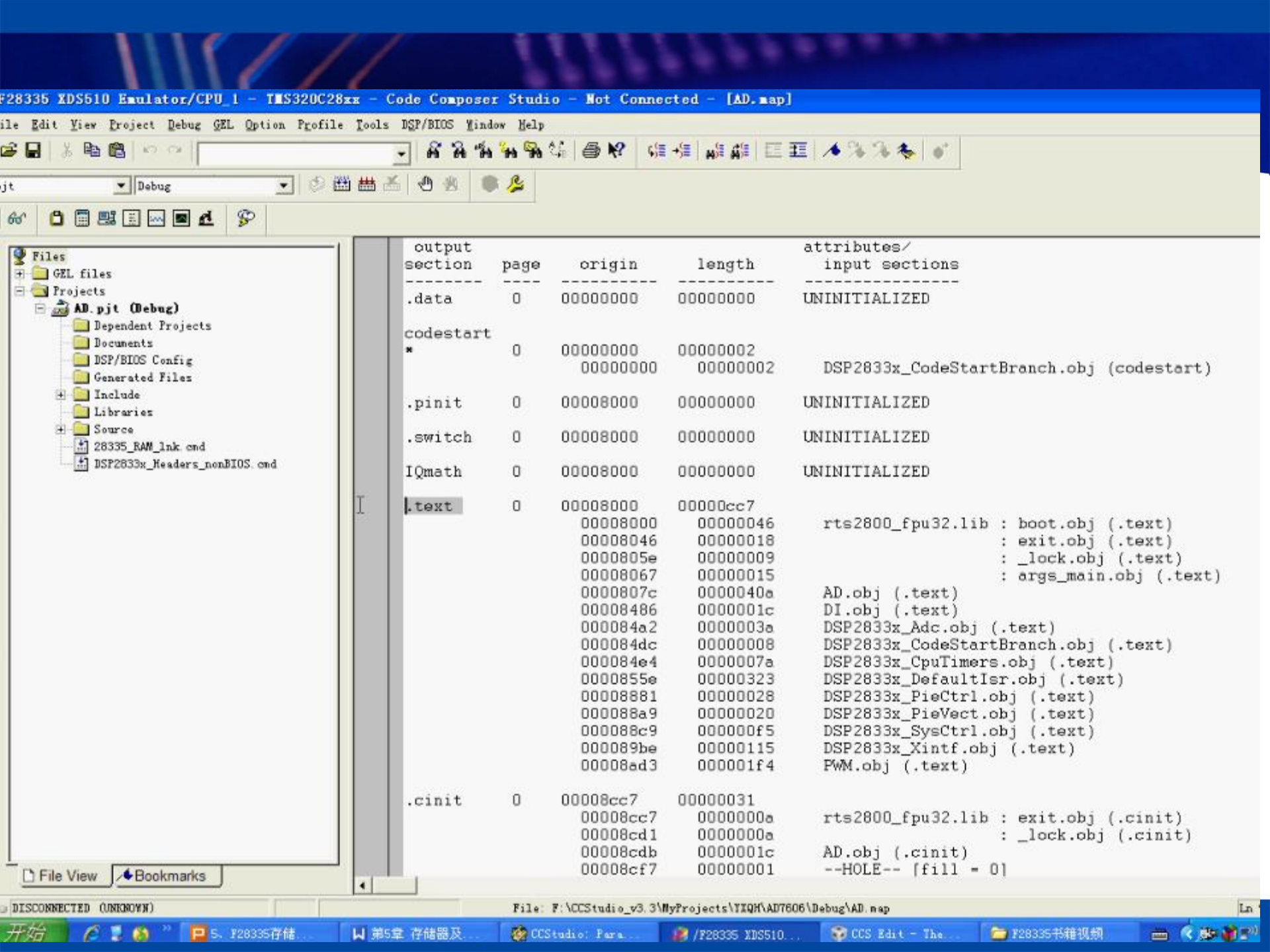
Files
GEL files
Projects
AD.pjt (Debug)
Dependent Projects
Documents
DSP/BIOS Config
Generated Files
Include
Libraries
Source
28335_RAM_lnk.cmd
DSP2833x_Headers_nonBIOS.cmd
File View
Bookmarks
TMS320C2000 COFF Linker PC v5.0.2
>> Linked Sun Mar 15 21:23:37 2015
OUTPUT FILE NAME: <./Debug/AD.out>
ENTRY POINT SYMBOL: "_c_int00" address: 00008000
MEMORY CONFIGURATION
name origin length used unused attr fill
PAGE 0:
BEGIN 00000000 00000002 00000002 00000000 RWIX
BOOT_RSVD 00000002 0000004e 00000000 0000004e RWIX
RAMM0 00000050 000003b0 00000000 000003b0 RWIX
RAML 00008000 00004000 00000d17 000032e9 RWIX
CSM_RSVD 0033ff80 00000076 00000000 00000076 RWIX
CSM_PWL 0033fff8 00000008 00000000 00000008 RWIX
ADC_CAL 00380080 00000009 00000007 00000002 RWIX
IQTABLES 003fe000 00000b50 00000000 00000b50 RWIX
IQTABLES2 003feb50 0000008c 00000000 0000008c RWIX
FPUTABLES 003febdc 000006a0 00000000 000006a0 RWIX
BOOTROM 003ff27c 00000d44 00000000 00000d44 RWIX
RESET 003fffc0 00000002 00000000 00000002 RWIX
PAGE 1:
RAMM 00000400 00000400 000003e8 00000018 RWIX
DEV_EMU 00000880 00000180 000000d0 000000b0 RWIX
FLASH_REGS 00000a80 00000060 00000008 00000058 RWIX
CSM 00000ae0 00000010 00000010 00000000 RWIX
ADC_MIRROR 00000b00 00000010 00000010 00000000 RWIX
XINTF 00000b20 00000020 0000001e 00000002 RWIX
CPU_TIMER0 00000c00 00000008 00000008 00000000 RWIX
CPU_TIMER1 00000c08 00000008 00000008 00000000 RWIX
CPU_TIMER2 00000c10 00000008 00000008 00000000 RWIX
DISCONNECTED (UNKNOWN)
File: F:\CCStudio_v3.3\MyProjects\YIQM\AD7606\Debug\AD.map
开始
5、F28335存储...
第5章 存储器及...
CCStudio: Para...
/F28335 XDS510...
CCS Edit - The...
F28335书籍视频


F28335 XDS510 Emulator/CPU_1 - TMS320C28xx - Code Composer Studio - Not Connected - [AD.map]
File Edit View Project Debug GEL Option Profile Tools DSP/BIOS Window Help
Debug
Files
GEL files
Projects
AD.pjt (Debug)
Dependent Projects
Documents
DSP/BIOS Config
Generated Files
Include
Libraries
Source
28335_RAM_lnk.cmd
DSP2833x_Headers_nonBIOS.cmd
File View
Bookmarks
output section page origin length attributes/ input sections
.data 0 00000000 00000000 UNINITIALIZED
codestart
* 0 00000000 00000002
00000000 00000002 DSP2833x_CodeStartBranch.obj (codestart)
.pinit 0 00008000 00000000 UNINITIALIZED
.switch 0 00008000 00000000 UNINITIALIZED
IQmath 0 00008000 00000000 UNINITIALIZED
.text 0 00008000 00000cc7
00008000 00000046 rts2800_fpu32.lib : boot.obj (.text)
00008046 00000018 : exit.obj (.text)
0000805e 00000009 : _lock.obj (.text)
00008067 00000015 : args_main.obj (.text)
0000807c 0000040a AD.obj (.text)
00008486 0000001c DI.obj (.text)
000084a2 0000003a DSP2833x_Adc.obj (.text)
000084dc 00000008 DSP2833x_CodeStartBranch.obj (.text)
000084e4 0000007a DSP2833x_CpuTimers.obj (.text)
0000855e 00000323 DSP2833x_DefaultIsr.obj (.text)
00008881 00000028 DSP2833x_PieCtrl.obj (.text)
000088a9 00000020 DSP2833x_PieVect.obj (.text)
000088c9 000000f5 DSP2833x_SysCtrl.obj (.text)
000089be 00000115 DSP2833x_Xintf.obj (.text)
00008ad3 000001f4 PWM.obj (.text)
.cinit 0 00008cc7 00000031
00008cc7 0000000a rts2800_fpu32.lib : exit.obj (.cinit)
00008cd1 0000000a : _lock.obj (.cinit)
00008cdb 0000001c AD.obj (.cinit)
00008cf7 00000001 --HOLE-- [fill = 0]
DISCONNECTED (UNKNOWN)
File: F:\CCStudio_v3.3\MyProjects\YIQH\AD7606\Debug\AD.map
开始
S. F28335存储...
第5章 存储器及...
CCStudio: Para...
/F28335 XDS510...
CCS Edit - The...
F28335书籍视频

第五讲：存储器以及地址分配

1、TMS320F28335存储器空间分配

2、TMS320F28335存储器保护特点

3、XINTF接口

4、相关寄存器介绍

XINTF接口

当F288335片上存储器不够用时，需要进一步扩展，外部接口XINTF采用非复用一部总线，可用于扩展SRAM、FLASH、ADC、DAC模块等。XINTF接口分别映射到3个固定的存储器映射区域，模块的信号见图5.3。

XINTF每个区域都有一个片选信号线，当对某个区域进行读写访问时，就要将信号线置低，某些器件将两个区域的片选信号通过内部的与逻辑连接在一起，从而形成一个共用的信号线，在这样的情况下，同一存储器可以与两个XINTF区域相连，要区分这两个区域就要与区分这两个区域的逻辑电路相连。

Figure 1. External Interface Block Diagram

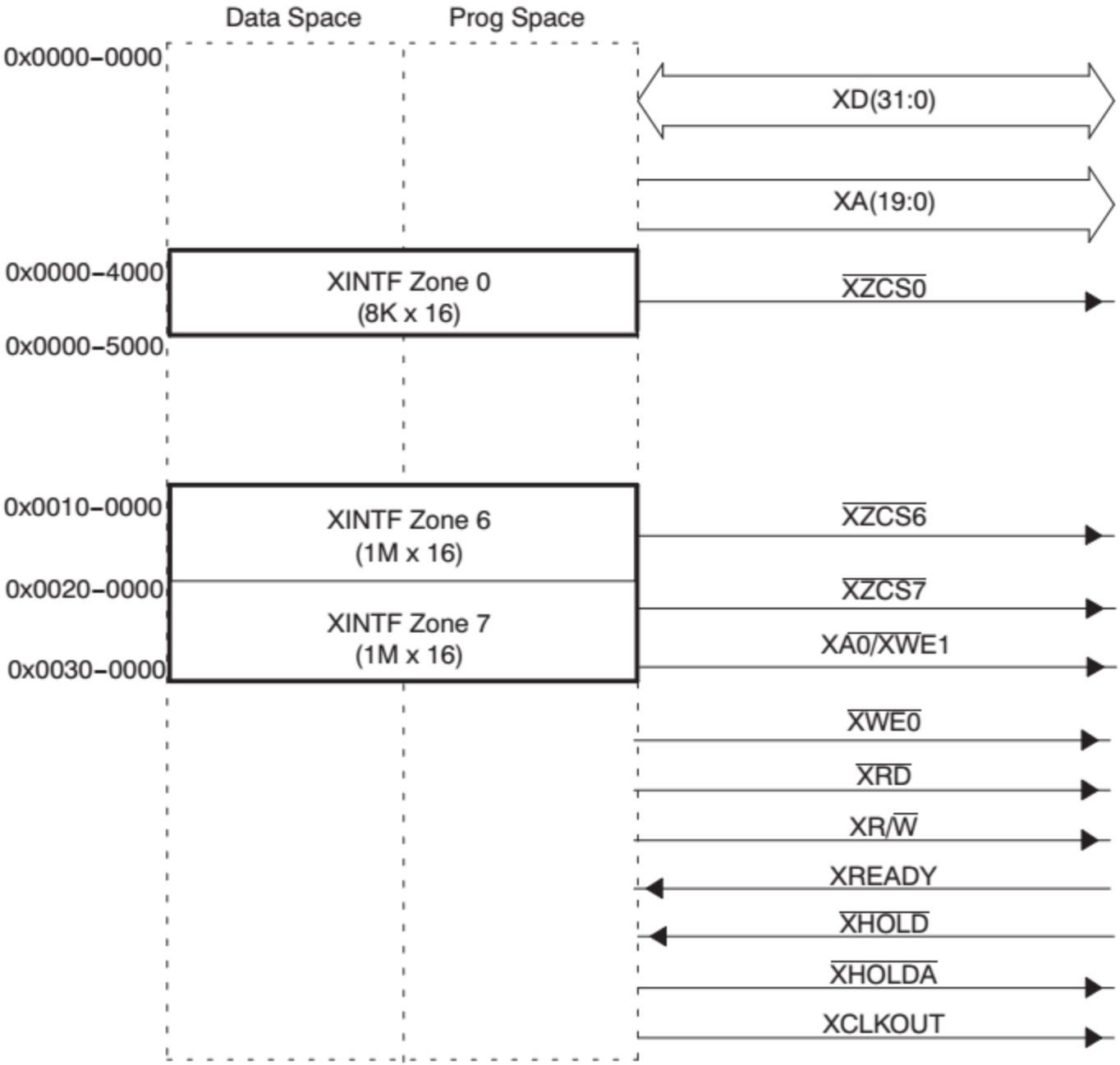


Table 13. XINTF Signal Descriptions

Name	Type	Description
XD(31:0)	I/O/Z	Bidirectional 32-bit data bus. In 16-bit mode only XD(15:0) are used.
XA(31:1)	O/Z	Address bus. The address is placed on the bus on the rising edge of XCLKOUT and held on the bus until the next access. Specific devices may not have all 32 address lines. See the data sheet for a specific device.
XA0/ $\overline{\text{XWE1}}$	O/Z	In 16-bit data mode (see), this signal is the least significant address line (XA0). In 32-bit data mode, this signal is the active low write strobe $\overline{\text{XWE1}}$. $\overline{\text{XWE1}}$ is used, along with $\overline{\text{XWE0}}$, for 32-bit bus operation as shown in Section 2.7.
XCLKOUT	O/Z	Single output clock derived from the XTIMCLK to be used for on-chip and off-chip wait-state generation and as a general-purpose clock source. XCLKOUT is either the same frequency or ½ the frequency of XTIMCLK, as defined by the CLKMODE bit in the XINTCNF2 register. At reset XCLKOUT = XTIMCLK/2 XTIMCLK = SYSCLKOUT/2
$\overline{\text{XWE0}}$	O/Z	Active low write strobe. In 16-bit mode, this signal is driven low on all bus modes and data size types. In 32-bit mode, it is driven as shown in Figure 5. The write strobe waveform is specified, per zone basis, by the Lead, Active, Trail periods in the XTIMINGx registers.

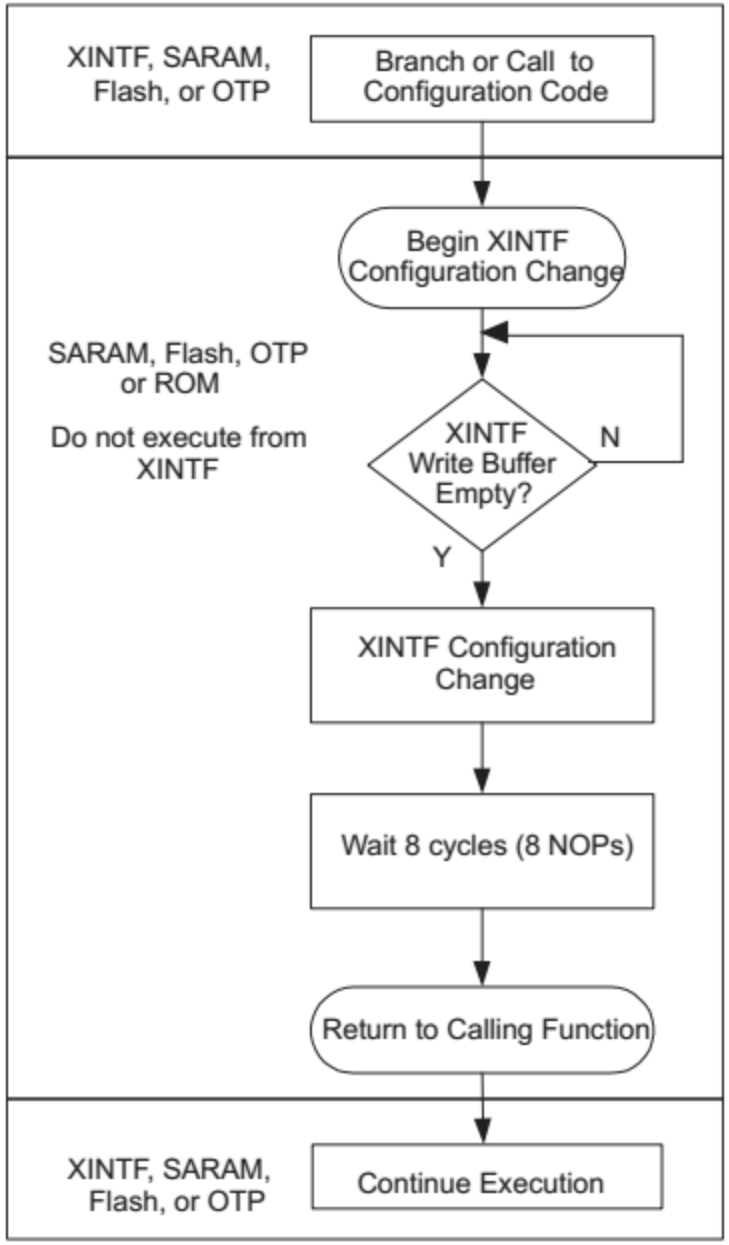
$\overline{\text{XRD}}$	O/Z	Active low read strobe. This signal is driven low on all bus modes and data size types. The read strobe waveform is specified, per zone basis, by the Lead, Active, Trail periods in the XTIMINGx registers. Note: The $\overline{\text{XRD}}$ and $\overline{\text{XWE0}}$ signals are mutually exclusive.
XR/$\overline{\text{W}}$	O/Z	Read-not-write control. When high, this signal indicates a read cycle is active, when low, it indicates a write cycle is active. This signal is normally held high. The XR/$\overline{\text{W}}$ signal performs similar functions to the $\overline{\text{XRD}}$ and $\overline{\text{XWE0}}$ signals. Generally, users opt to use $\overline{\text{XWE0}}$ and $\overline{\text{XWE1}}$ because they are cleaner and easier to use.
$\overline{\text{XZCS0}}$ $\overline{\text{XZCS6}}$ $\overline{\text{XZCS7}}$	O	Zone chip-selects. These signals are active when an access to the addressed zone is performed.
XREADY	I	Indicates peripheral is READY to complete the access when asserted to 1. For each XINTF zone, this can be configured to be a synchronous or an asynchronous input. In synchronous mode, the XINTF interface block requires XREADY to be valid one XTIMCLK clock cycle before the end of the active period. In asynchronous mode, The XINTF interface block samples XREADY three XTIMCLK clock cycles before the end of the active period. XREADY is sampled at the XTIMCLK rate independent of the XCLKOUT mode.
$\overline{\text{XHOLD}}$	I	This signal, when active low, requests the XINTF to release the external bus (place all busses and strobes into high-impedance state). The XINTF releases the bus when any current access is complete and there are no pending accesses on the XINTF. This signal is an asynchronous input and is synchronized by XTIMCLK.
$\overline{\text{XHOLDA}}$	O/Z	This signal is driven active low, when the XINTF has granted an $\overline{\text{XHOLD}}$ request. All XINTF busses and strobe signals will be in a high-impedance state. This signal is released when the $\overline{\text{XHOLD}}$ signal is released. External devices should only drive the external bus when this signal is active low.

XINTF接口

XINTF的存储器的3个区域中的任何一个都可通过编程设定独立的等待时间，选通信号建立时间及保持时间，每个区域的读写操作都可以配置成不同的等待时间.

另外可以通过XREADY信号线延长等待时间，XINTF接口的这些特性允许其访问不同速率的外部存储器设备。通过XTIMINGx寄存器可配置每个区域的等待时间及选通信号的建立于保持时间。XINTF接口的访问时序是以内部时钟XTIMCLK为基准的，XTIMCLK信号频率可配置为系统时钟SYSCLKOUT的频率或其一半。

Figure 2. Access Flow Diagram



Branch or call is required to properly flush the CPU pipeline before the configuration change.

The function that changes the configuration cannot execute from the XINTF.

The XINTF write buffer must be empty before the configuration change.

The stack must not be in external memory.

Write instructions to XTIMING0/6/7, XBANK, or XINTCNF2

Wait eight cycles to let the write instructions propogate through the CPU pipeline. This must be done before the return-from-function call is made.

Figure 3. Relationship Between XTIMCLK and SYSCLKOUT

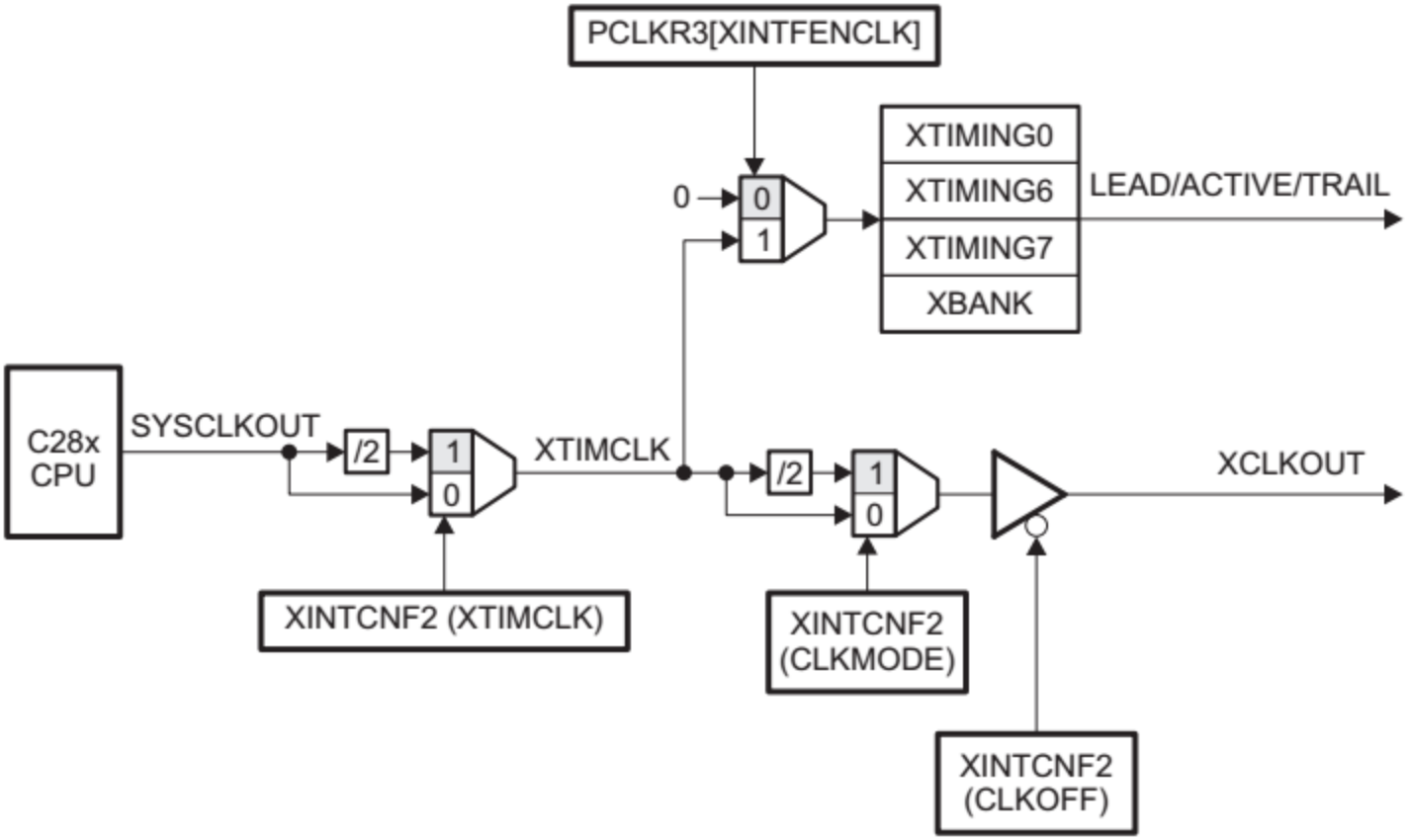


Figure 11. XTIMCLK and XCLKOUT Mode Waveforms

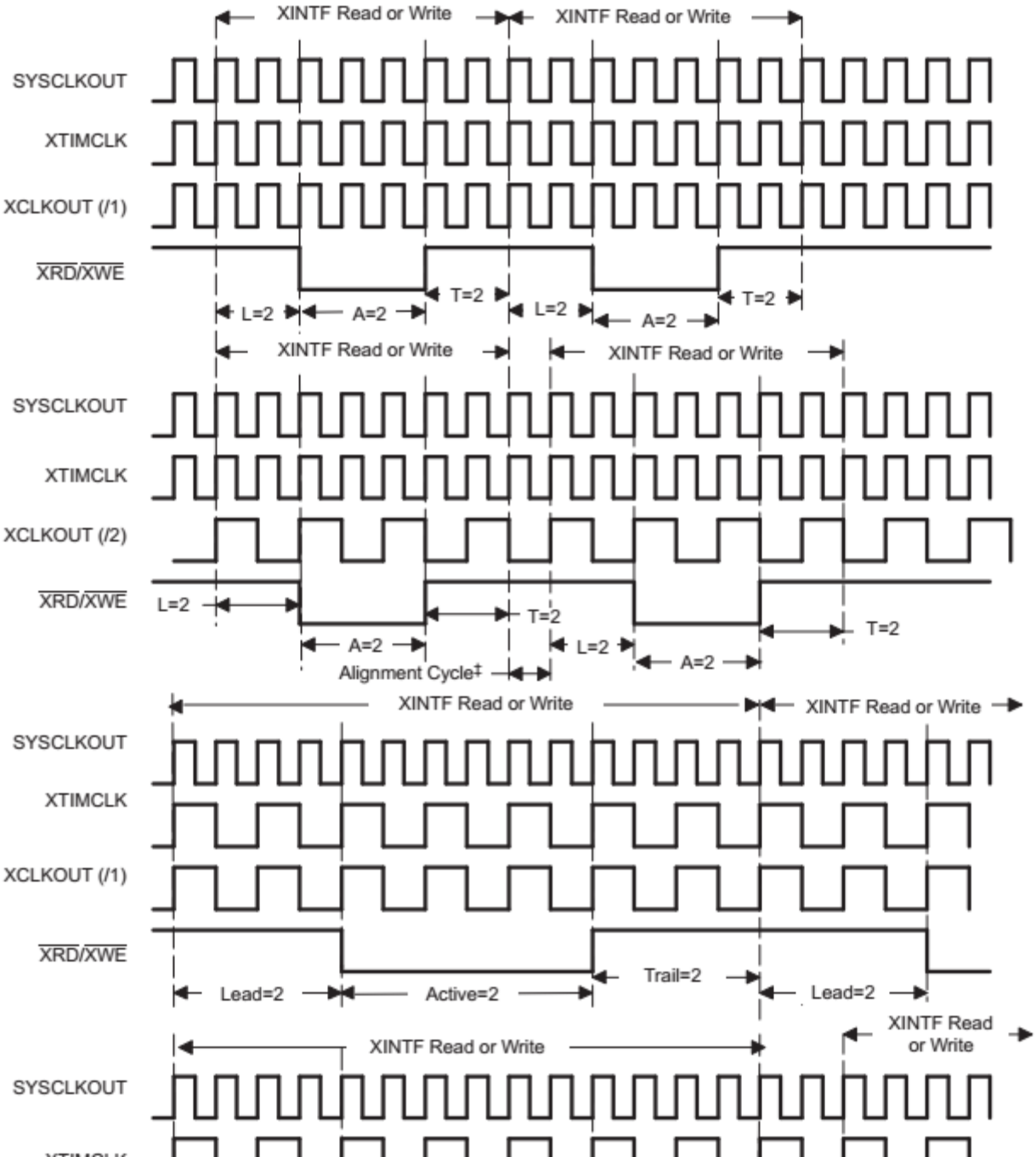
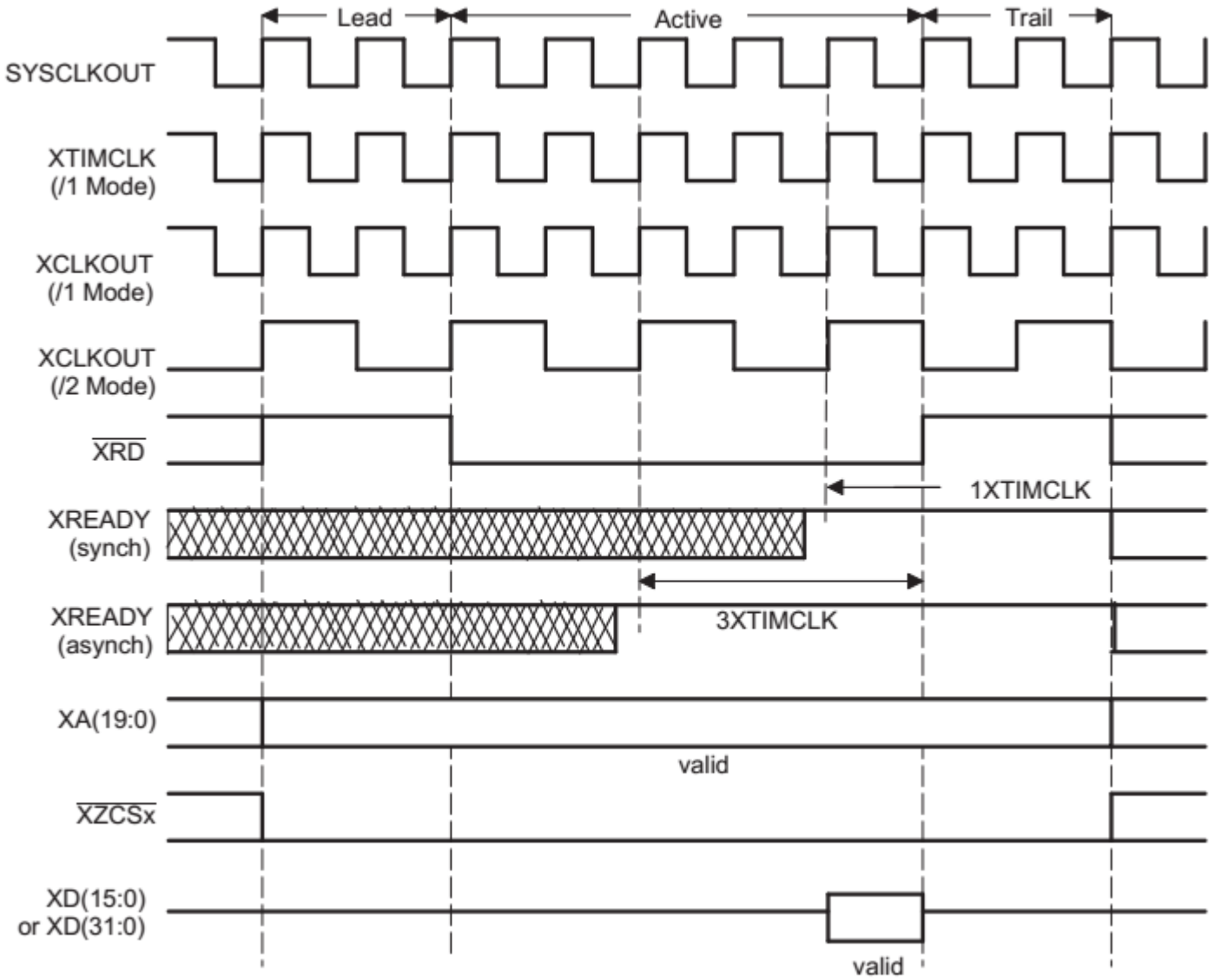
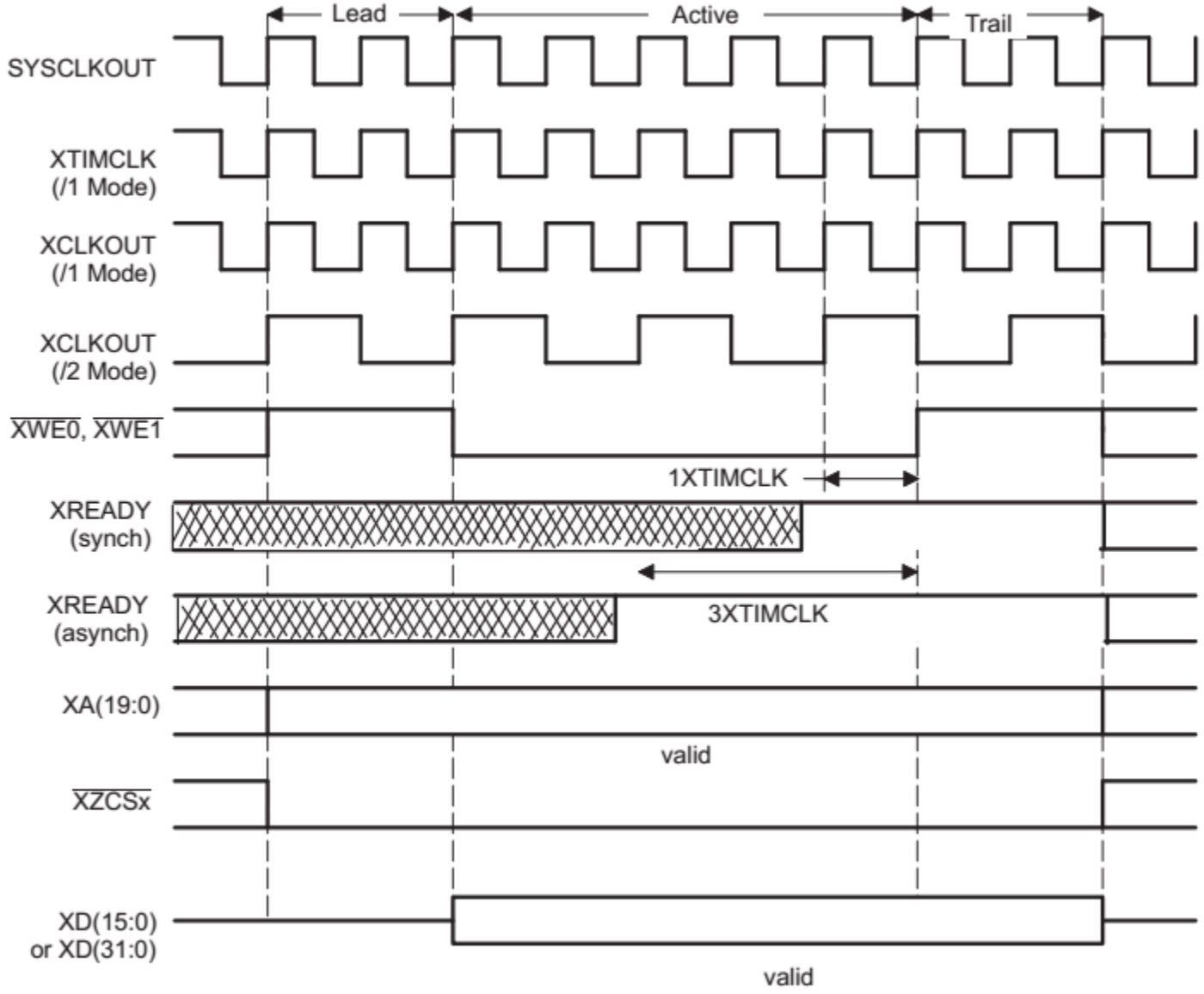


Figure 12. Generic Read Cycle (XTIMCLK = SYSCLKOUT mode)



A XRDLEAD = 2, XRDACTIVE = 4, XRDTRAIL = 2

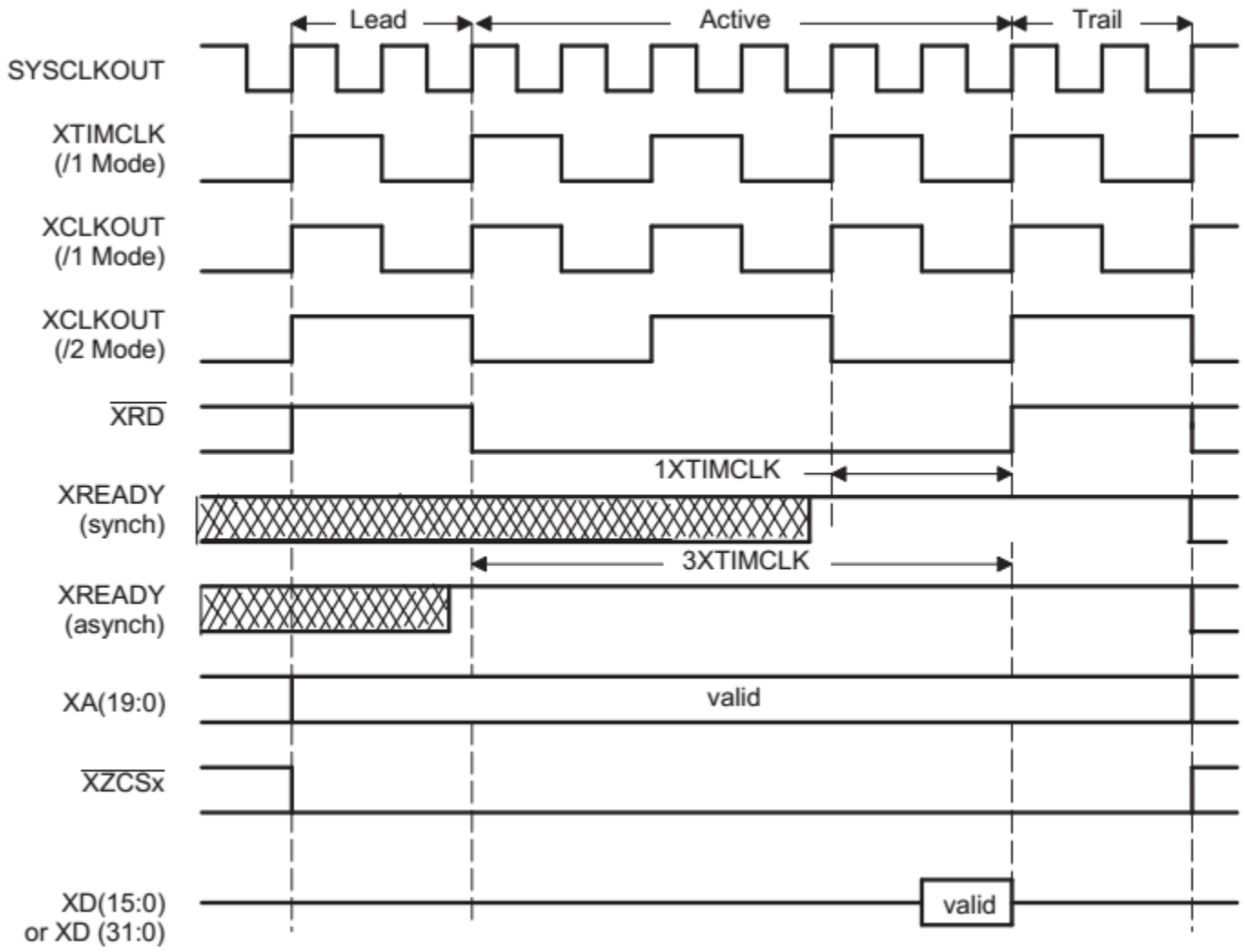
Figure 14. Generic Write Cycle (XTIMCLK = SYSCLKOUT mode)



A XWRACTIVE = 2, XWRACTIVE = 4, XWRTRAIL = 2

B If the lead and active timing parameters are set low enough, it may not be possible to generate a valid XREADY signal. No hardware is added to detect this.

Figure 13. Generic Read Cycle (XTIMCLK = ½ SYSCLKOUT mode)



A XRDLEAD = 1, XRDACTIVE = 3, XRDTRAIL = 1

Figure 4. Typical 16-bit Data Bus XINTF Connections

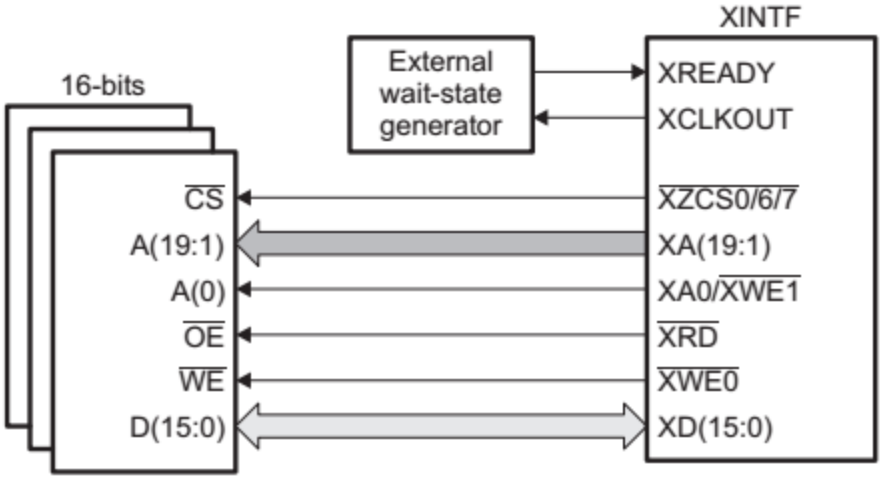


Figure 5. Typical 32-bit Data Bus XINTF Connections

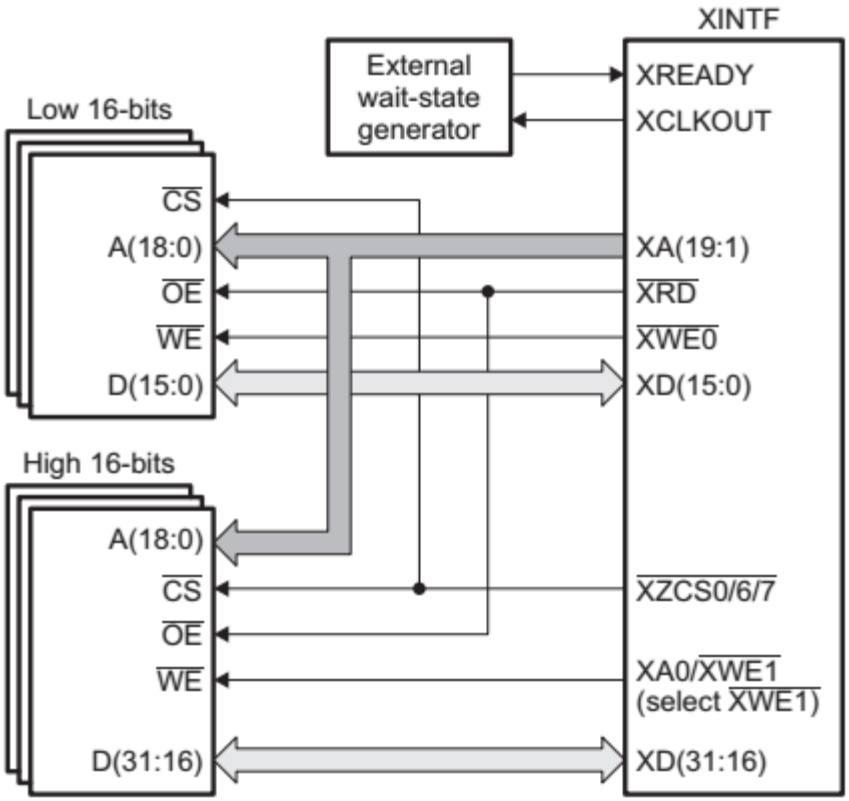


Table 7. XINTF Configuration and Control Register Mapping

Name	Address	Size (x16)	Description [1]
XTIMING0	0x0000−0B20	2	XINTF Timing Register, Zone 0
XTIMING6[2]	0x0000−0B2C	2	XINTF Timing Register, Zone 6
XTIMING7	0x0000−0B2E	2	XINTF Timing Register, Zone 7
XINTCNF2[3]	0x0000−0B34	2	XINTF Configuration Register
XBANK	0x0000−0B38	1	XINTF Bank Control Register
XREVISION	0x0000−0B3A	1	XINTF Revision Register
XRESET	0x0000 083D	1	XINTF Reset Register

(1) All XINTF registers are EALLOW protected.

(2) XTIMING1 - XTIMING5 are reserved for future expansion and are not currently used.

(3) XINTCNF1 is reserved and not currently used.

Figure 6. XTIMING0/6/7 Register

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved									X2TIMING	Reserved				XSIZE	
R-0									R/W-1	R-0				R/W-1	

15	14	13	12	11	10	9	8
READYMODE	USEREADY	XRDLEAD		XRDACTIVE			XRDTRAIL
R/W-1	R/W-1	R/W-1		R/W-1			R/W-1

7	6	5	4	3	2	1	0
XRDTRAIL	XWRLEAD	XWRACTIVE				XWRTRAIL	
R/W-1	R/W-1	R/W-1					

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. XTIMING0/6/7 Register Field Descriptions

Bit	Field	Value	Description (1)
31:23	Reserved	0	
22	X2TIMING		This bit specifies the scaling factor of the XRDLEAD, XRDACTIVE, XRDTRAIL, XWRLEAD, XWRACTIVE, and XWRTRAIL values for the zone.
		0	The values are scaled 1:1
		1	The values are scaled 2:1 (doubled). This the default mode of operation on power up and reset.
21:18	Reserved	0	
17:16	XSIZE		These two bits must always be written to as either 0, 1 (32-bit data bus) or 1, 1 (16-bit data bus). Any other combination is reserved and will result in incorrect XINTF behavior.
		00	Reserved - results in incorrect XINTF behavior
		01	32-bit interface. In this mode the zone will use all 32 data lines. The XA0/$\overline{WE1}$ signal will behave as $\overline{WE1}$ as described in Section 2.7 .
		10	Reserved - results in incorrect XINTF behavior
		11	16-bit interface. In this mode the zone will only use 16 data lines. The XA0/$\overline{WE1}$ signal will behave as XA0. (default at reset)
15	READYMODE		Sets the XREADY input sampling for the zone as synchronous or asynchronous. This bit is ignored if XREADY is not sampled (USEREADY = 0).
		0	XREADY input is synchronous for the zone.
		1	XREADY input is asynchronous for the zone. (default at reset)
14	USEREADY		Determines if accesses to the zone will sample or ignore the XREADY input signal.
		0	The XREADY signal is ignored when accesses are made to the zone.
		1	The XREADY signal can further extend the active portion of an access to the zone past the minimum defined by the XRDACTIVE and XWRACTIVE fields.

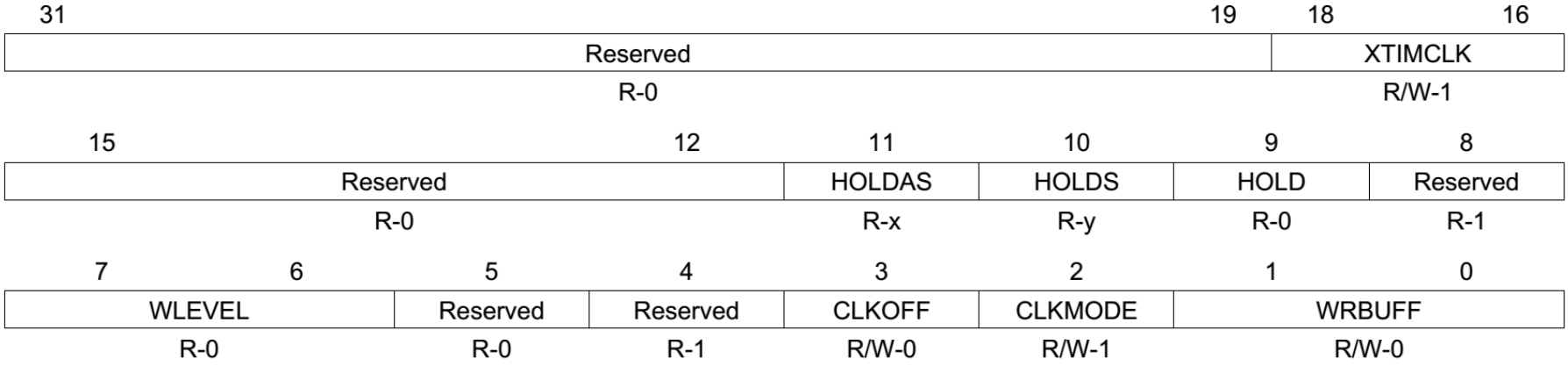
<table>
<tr><td>13:12</td><td>XRDLEAD</td><td></td><td colspan="2">Two-bit field that defines the read cycle lead wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled.
See Section 4 for minimum requirements in different modes.</td></tr>
<tr><td></td><td></td><td></td><td>X2TIMING</td><td>Read Lead Period</td></tr>
<tr><td></td><td></td><td>00</td><td>X</td><td>Invalid</td></tr>
<tr><td></td><td></td><td>01</td><td>0</td><td>1 XTIMCLK cycle</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>2 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>10</td><td>0</td><td>2 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>4 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>11</td><td>0</td><td>3 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>6 XTIMCLK cycles (default)</td></tr>
<tr><td>11:9</td><td>XRDACTIVE</td><td></td><td colspan="2">Three-bit field that defines the read cycle active wait state period, in XTIMCLK cycles. The active period is by default 1 XTIMCLK cycle. Therefore, the total active period is (1 + XWRACTIVE) XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled.
See Section 4 for minimum requirements in different modes.</td></tr>
<tr><td></td><td></td><td></td><td>X2TIMING</td><td>Read Active Period Waitstates</td></tr>
<tr><td></td><td></td><td>000</td><td>0</td><td>0</td></tr>
<tr><td></td><td></td><td>001</td><td>0</td><td>1 XTIMCLK cycle</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>2 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>010</td><td>0</td><td>2 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>4 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>011</td><td>0</td><td>3 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>6 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>100</td><td>0</td><td>4 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>8 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>101</td><td>0</td><td>5 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>10 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>110</td><td>0</td><td>6 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td></td><td>1</td><td>12 XTIMCLK cycles</td></tr>
<tr><td></td><td></td><td>111</td><td>0</td><td>7 XTIMCLK cycles</td></tr>
</table>

8:7	XRDTRAIL		Two-bit field that defines the read cycle trail wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Read Trail Period**
		00	0	0
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)
6:5	XWRLEAD		Two-bit field that defines the write cycle lead wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Write Lead Period**
		00	0	0
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)

4:2	XWRACTIVE		Three-bit field that defines the write cycle active wait state period, in XTIMCLK cycles. The active period is by default 1 XTIMCLK cycle. Therefore, the total active period is (1 + XWRACTIVE) XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Write Active Period Waitstates**
		000	0	0
		001	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		010	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		011	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles
		100	0	4 XTIMCLK cycles
			1	8 XTIMCLK cycles
		101	0	5 XTIMCLK cycles
			1	10 XTIMCLK cycles
		110	0	6 XTIMCLK cycles
			1	12 XTIMCLK cycles
		111	0	7 XTIMCLK cycles
			1	14 XTIMCLK cycles (default)

1:0	XWRTRAIL		Two-bit field that defines the write cycle trail wait state period, in XTIMCLK cycles. If the X2TIMING bit is set, then the number of wait states are doubled. See Section 4 for minimum requirements in different modes.	
			X2TIMING	**Write Trail Period**
		00	x	
		01	0	1 XTIMCLK cycle
			1	2 XTIMCLK cycles
		10	0	2 XTIMCLK cycles
			1	4 XTIMCLK cycles
		11	0	3 XTIMCLK cycles
			1	6 XTIMCLK cycles (default)

Figure 7. XINTF Configuration Register (XINTCNF2)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset/ x = $\overline{\text{XHOLDA}}$ output; y = $\overline{\text{XHOLD}}$ input

Figure 8. XBANK Register

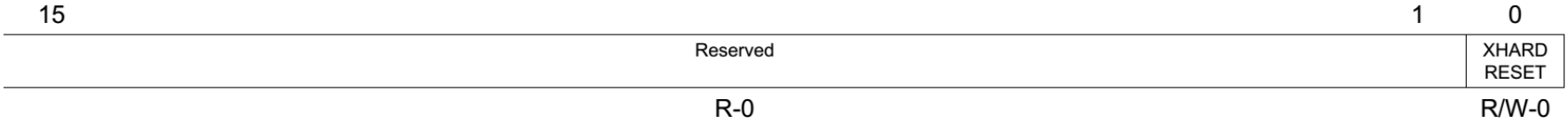
15	6	5	3	2	0
Reserved		BCYC		BANK	
R-0		R/w-1		R/W-1	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. XBANK Register Field Descriptions

Bit	Field	Value	Description [1]
15:6	Reserved		
5:3	BCYC		These bits specify the number of XTIMCLK cycles to add between any consecutive access that crosses into or out of the specified zone, be it a read or write, program or data space. The number of XTIMCLK cycles can be 0 to 7. On a reset ($\overline{\text{XRS}}$), the value defaults to 7 XTIMCLK cycles (14 SYSCLKOUT cycles).
		000	0 cycle
		001	1 XTIMCLK cycle
		010	2 XTIMCLK cycles
		011	3 XTIMCLK cycles
		100	4 XTIMCLK cycles
		101	5 XTIMCLK cycles
		110	6 XTIMCLK cycles
		111	7 XTIMCLK cycles (default)
2:0	BANK		These bits specify the XINTF zone for which bank switching is enabled, ZONE 0 to ZONE 7. At reset, XINTF Zone 7 is selected.
		000	Zone 0
		001	Reserved
		010	Reserved
		011	Reserved
		100	Reserved
		101	Reserved
		110	Zone 6
		111	Zone 7 (selected at reset by default)

Figure 10. XRESET Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. XRESET Register Field Descriptions

Bit	Field	Value	Description (1)
31	Reserved		
30	XHARDRESET		A hard reset may be used in cases where the CPU detects the XREADY signal is stuck low during a DMA transfer.
		0	Writing a 0 has no effect. This bit always reads back a 0.
		1	Force an XINTF hard reset. The XTIMING, XBANK, and XINTCNF2 registers will return to their default state and all XINTF signals will go to their inactive state. Any pending access will be lost including data in the write buffer. Any stall condition to DMA will be released.

(1) This register is EALLOW protected.

外扩SRAM硬件原理：

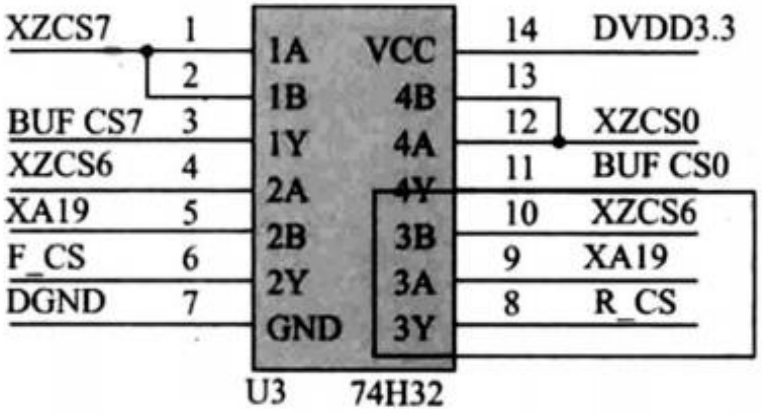
F28335 在逻辑上有 4M×16 位的程序空间和 4M×16 位的数据空间，但在物理上已将程序空间和数据空间统一成一个 4M×16 位的空间。尽管 TMS320F28335 片上有 256K×16 位 FLASH 存储器，34K×16 位单周期单次访问随机存储器的 SARAM，8K×16 位的 BOOT ROM，1K×16 位的 OTP ROM，但有可能运行程序的开销大于片上提供的这些资源，所以需要外扩。

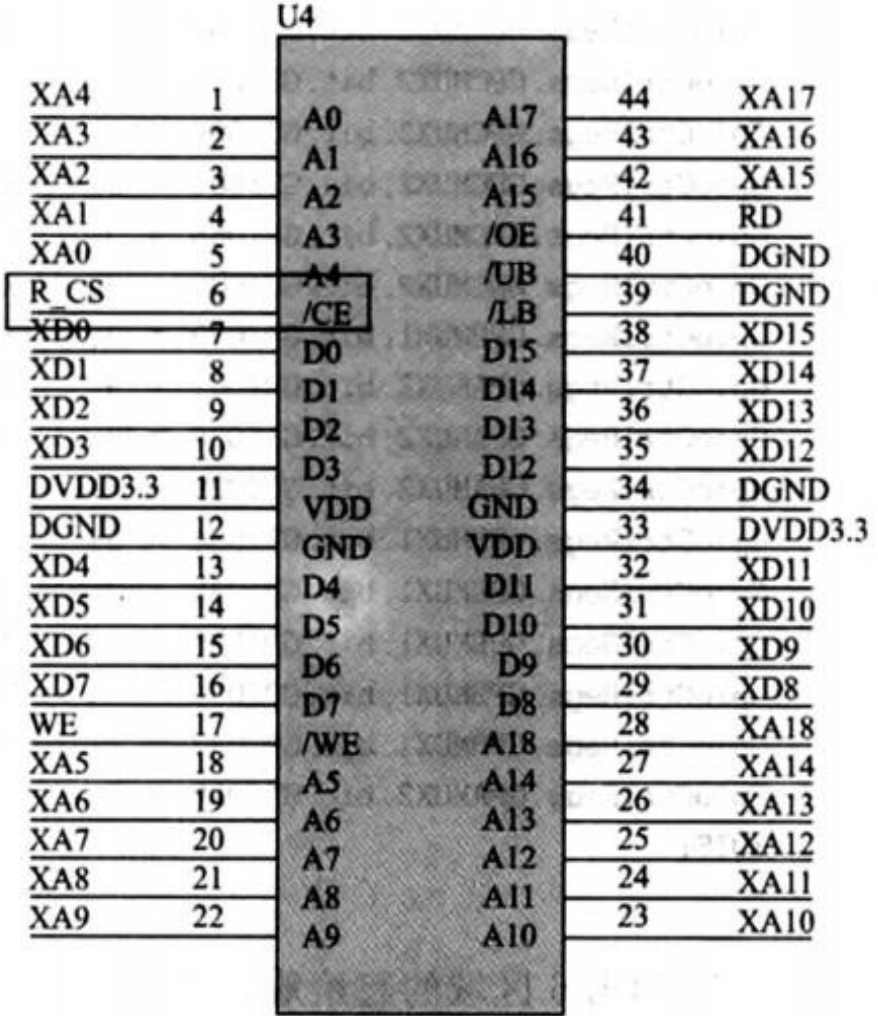
F28335 的外部存储器可以映射到 3 个存储区域，Zone0，Zone6 和 Zone7。

- Zone0 存储区域：0X004000～0X004FFF，4K×16 位可编程最少一个等待周期。
- Zone6 存储区域：0X100000～0X1FFFFF，1M×16 位 10 ns 最少一个等待周期。
- Zone7 存储区域：0X200000～0X2FFFFF，1M×16 位 70 ns 最少一个等待周期。

XA0:XA18：接DSP地址线　　XD0:XD15:接DSP数据线

XZCS6和地址线19通过74HC32与或后送给SRAM的片选信号实现将8M的SRAM映射到Zone6的前半部分。





呢？在外扩 RAM 电路设计好后，仿真时程序就可以导入外扩的 RAM 中进行，空间一般能够满足开发的需求，这样程序的设计和调试就非常方便。将程序下载到哪个空间，完全取决于 CMD 文件中对程序和数据空间的分配，关于 CMD 文件在后面的章节中会进行详细的介绍。

ISSI的IS62LV51216是一个8M容量，结构为512K*16位字长的高速率SRAM。IS62LV51216采用ISSI公司的高性能CMOS工艺制造。高度可靠的工艺水准加上创新的电路设计技术，使得IS61LV6416的存取时间可快至8ns，兼具低功耗的优点。

当/CE处于高电平（未选中）时，IS62LV51216进入待机模式。 在此模式下，功耗可降低至CMOS输入标准。

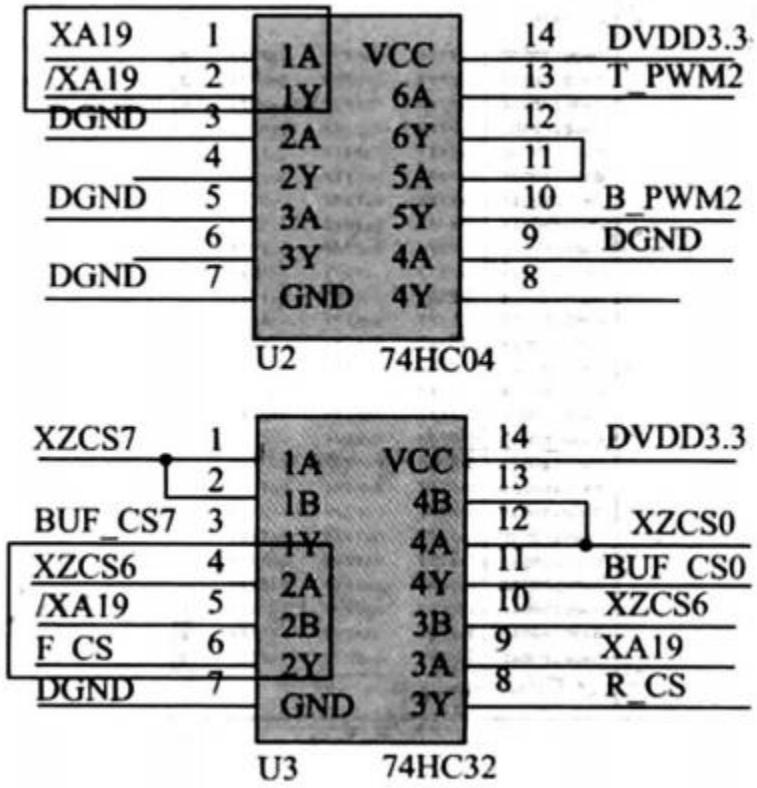
使用IS62LV51216的低触发片选引脚（/CE）和输出使能引脚（/OE），可以轻松实现存储器扩展。低触发写入使能引脚（/WE）将完全控制存储器的写入和读取。 同一个字节允许高位（/UB）存取和低位（/LB）存取。

IS62LV51216真值表

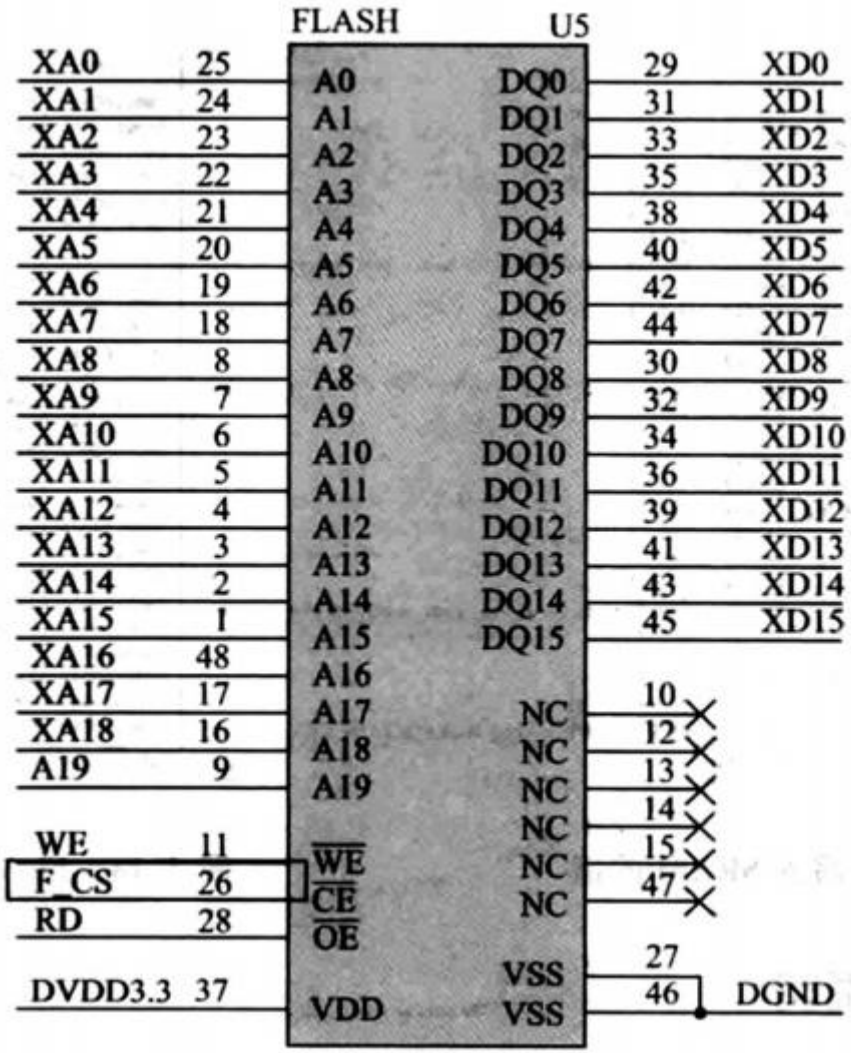
TRUTH TABLE

Mode	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O PIN I/O0-I/O7	I/O PIN I/O8-I/O15	V_{DD} Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

F28335片上有256K × 16 位的FLASH存储空间，如果在DSP中所编译的代码段高于Flash的存储容量，则需要外扩Flash空间来稳定地实现其功能。外扩FLASH的原理与外扩RAM 的原理一样，电路图如下所示



FLASH 外扩片选



FLASH 引脚接线

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```
// running outside of the XINTF.

// All Zones---------------------------------
// Timing for all zones based on XTIMCLK = 1/2 SYSCLKOUT
EALLOW;
XintfRegs.XINTCNF2.bit.XTIMCLK = 0;
// No write buffering
XintfRegs.XINTCNF2.bit.WRBUFF = 0;
// XCLKOUT is enabled
XintfRegs.XINTCNF2.bit.CLKOFF = 0;
// XCLKOUT = XTIMCLK/2
XintfRegs.XINTCNF2.bit.CLKMODE = 0;


// Zone 0------------------------------------
// When using ready, ACTIVE must be 1 or greater
// Lead must always be 1 or greater
// Zone write timing
XintfRegs.XTIMING0.bit.XWRLEAD = 3;
XintfRegs.XTIMING0.bit.XWRACTIVE = 3;
XintfRegs.XTIMING0.bit.XWRTRAIL = 3;
// Zone read timing
XintfRegs.XTIMING0.bit.XRDLEAD = 1;
XintfRegs.XTIMING0.bit.XRDACTIVE = 3;
XintfRegs.XTIMING0.bit.XRDTRAIL = 1;

// double all Zone read/write lead/active/trail timing
XintfRegs.XTIMING0.bit.X2TIMING = 1;

// Zone will sample XREADY signal
XintfRegs.XTIMING0.bit.USEREADY = 0;
XintfRegs.XTIMING0.bit.READYMODE = 0;  // sample asynchronous

// Size must be either:
// 0,1 = x32 or
// 1,1 = x16 other values are reserved
XintfRegs.XTIMING0.bit.XSIZE = 3;
```

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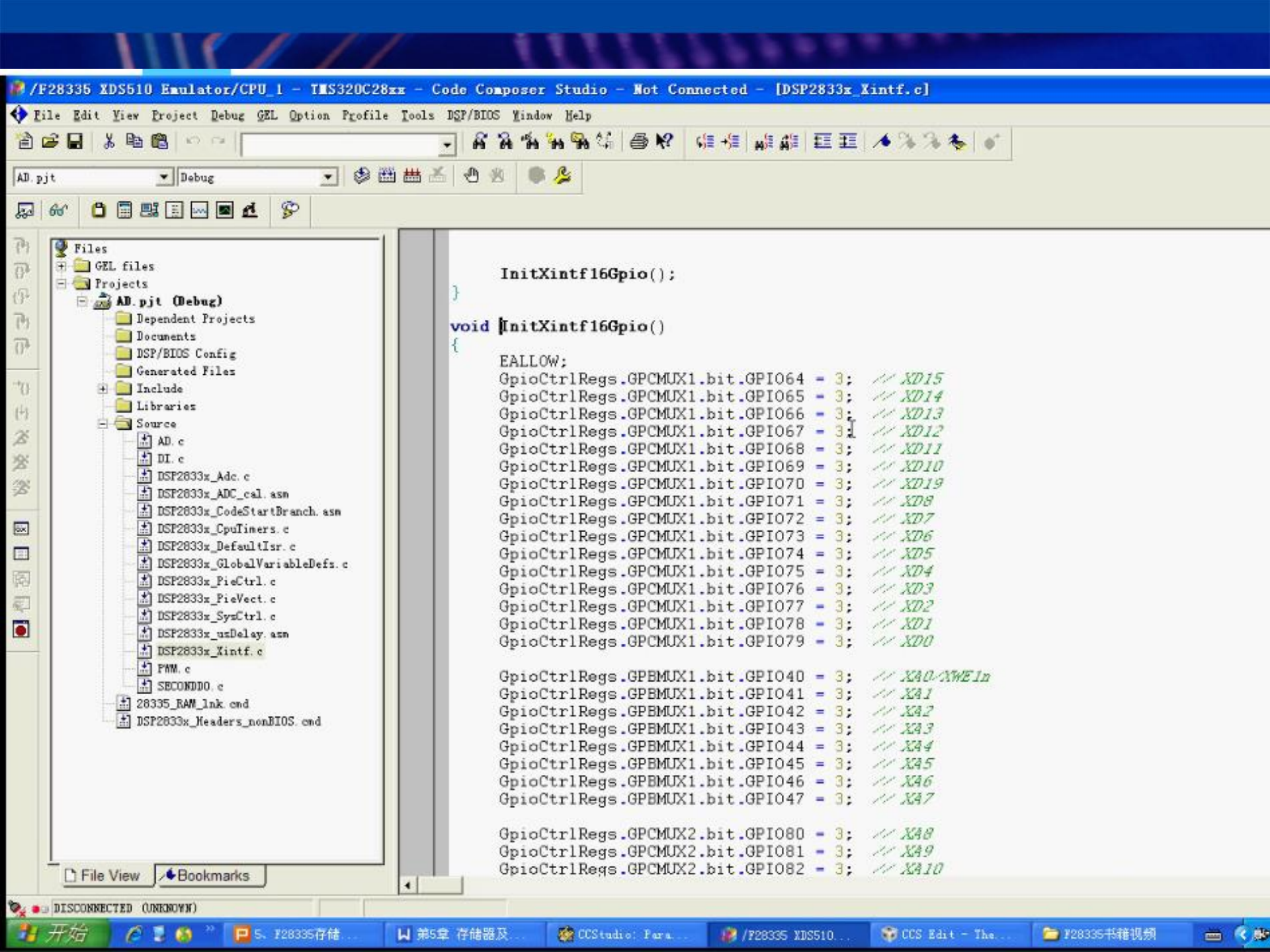
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InitXintf16Gpio();
}
void InitXintf16Gpio()
{
EALLOW;
GpioCtrlRegs.GPCMUX1.bit.GPIO64 = 3; // XD15
GpioCtrlRegs.GPCMUX1.bit.GPIO65 = 3; // XD14
GpioCtrlRegs.GPCMUX1.bit.GPIO66 = 3; // XD13
GpioCtrlRegs.GPCMUX1.bit.GPIO67 = 3; // XD12
GpioCtrlRegs.GPCMUX1.bit.GPIO68 = 3; // XD11
GpioCtrlRegs.GPCMUX1.bit.GPIO69 = 3; // XD10
GpioCtrlRegs.GPCMUX1.bit.GPIO70 = 3; // XD19
GpioCtrlRegs.GPCMUX1.bit.GPIO71 = 3; // XD8
GpioCtrlRegs.GPCMUX1.bit.GPIO72 = 3; // XD7
GpioCtrlRegs.GPCMUX1.bit.GPIO73 = 3; // XD6
GpioCtrlRegs.GPCMUX1.bit.GPIO74 = 3; // XD5
GpioCtrlRegs.GPCMUX1.bit.GPIO75 = 3; // XD4
GpioCtrlRegs.GPCMUX1.bit.GPIO76 = 3; // XD3
GpioCtrlRegs.GPCMUX1.bit.GPIO77 = 3; // XD2
GpioCtrlRegs.GPCMUX1.bit.GPIO78 = 3; // XD1
GpioCtrlRegs.GPCMUX1.bit.GPIO79 = 3; // XD0
GpioCtrlRegs.GPBMUX1.bit.GPIO40 = 3; // XA0/XWE1n
GpioCtrlRegs.GPBMUX1.bit.GPIO41 = 3; // XA1
GpioCtrlRegs.GPBMUX1.bit.GPIO42 = 3; // XA2
GpioCtrlRegs.GPBMUX1.bit.GPIO43 = 3; // XA3
GpioCtrlRegs.GPBMUX1.bit.GPIO44 = 3; // XA4
GpioCtrlRegs.GPBMUX1.bit.GPIO45 = 3; // XA5
GpioCtrlRegs.GPBMUX1.bit.GPIO46 = 3; // XA6
GpioCtrlRegs.GPBMUX1.bit.GPIO47 = 3; // XA7
GpioCtrlRegs.GPCMUX2.bit.GPIO80 = 3; // XA8
GpioCtrlRegs.GPCMUX2.bit.GPIO81 = 3; // XA9
GpioCtrlRegs.GPCMUX2.bit.GPIO82 = 3; // XA10
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```
#include "DSP2833x_Device.h"     // DSP2833x Headerfile Include File
#include "DSP2833x_Examples.h"   // DSP2833x Examples Include File
//////////////////////////////PWM频率初始化函数//////////////////////////////////////
//     chanel:PWM通道数                                                        //
//     prd: PWM周期值       f=50mhz/prd*2                                      //
//     同时保证有波形，将比较寄存器设为50%                                      //
////////////////////////////////////////////////////////////////////////////////
void PWMPRDInit(Uint16 chanel,Uint16 prd)
{

    switch(chanel)
    {
     case 1:pwmprd1=prd;
            #define pwmprd1 *(Uint16*)0x204002
            break;
     case 2:pwmprd2=prd;
            pwmduty2=prd * 0.5;
            break;
     case 3:pwmprd3=prd;
            pwmduty3=prd * 0.5;
            break;
     case 4:pwmprd4=prd;
            pwmduty4=prd * 0.5;
            break;
     case 5:pwmprd5=prd;
            pwmduty5=prd * 0.5;
            break;
     case 6:pwmprd6=prd;
            pwmduty6=prd * 0.5;
            break;
     case 7:pwmprd7=prd;
            pwmduty7=prd * 0.5;
            break;
     case 8:pwmprd8=prd;
            pwmduty8=prd * 0.5;
            break;
     case 9:pwmprd9=prd;
```

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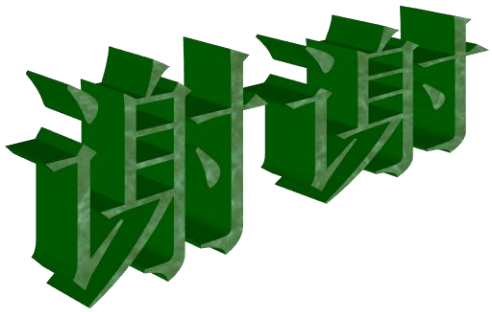
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